Low Power Current Mirror Topologies in 32nm Technology for VlSI Analog Circuit

Aman Kumar, Gurinder Pal Singh

Abstract- ***This paper deals with the analog circuit constructed using a current mirror. Two stage op-amp circuits are made from current mirror and other elements like source amplifier. Here, we have constructed four types of current mirror named as Conventional CM, Cascode CM, Wilson CM, modified Wilson CM. The imperative constraints of current mirrors approaches are source voltage for small power, output resistance, overall power, constancy are related to each other. On studying these schemes, it is detected that modified Wilson current mirror current mirror system has increased the output resistance by 21MΩ to 37MΩ of the Wilson current mirror and decreased the power consumption by 23.10µW to 19.43µW.We have also constructed two-stage op-amps with help of conventional current mirror. In this paper an operational amplifier by CMOS is presented whose input depends on bias current which is 20uA and designed using 32nm technology. In sub-threshold region due to unique behavior of the MOSFET transistors not only allows a designer to work at low voltage and also at low input bias current. Scaling of MOSFET and keeping V_{dd} up to 0.8V-1.2V gain and phase margin of purposed op-amp has been obtained 78.6db and 68.8^{o} respectively. These simulations are accomplished in 32nm CMOS technology using Galaxy cdesigner tool in Synopsis.***

Keywords: -Mixed design, CMOS, Two Stage op-amp, Current Mirrors, Synopsis, diode connected, MOSFET, Low voltage.

I. INTRODUCTION

The outlining of superior analog incorporated circuits is turning out to be most fundamental with the continuous trend towards the lessened supply voltages and transistor channel length. MOS is most accomplishment among all since it can be downsized to littler measurements for higher execution. The size can be diminished to micrometer or nanometer for getting higher execution. On downsizing the Transistor measure the most vital preferred standpoint is we can incorporate more number of transistor on a similar size and we can get a quicker intensifier contrasted with past one. This prompts to the ceaseless development of the handling limit per chip and working recurrence. Nowadays Current Mirrors (CM) are made by a method for CMOS innovation. It has emerged extensively and used in analog incorporated circuits. It goes about as biasing segments and additionally stacks gadgets for the enhanced stream. Usually, P- type MOS is used for current sink and the basic current radix is acknowledged with N-type MOS [1,2]. In the vast majority of the hardware circuits the current mirror is the most well-known building module.

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So as the transistor channel length and power supply is decreased then the outline of current mirror confronts continuous challenge.

Because of various aspect ratios (W/L), different parameters are varies according to channel length. Sizing of the transistor is actual huge issue. At the transistor level, execution of a current mirror is very important according to aspect ratio. In real life mirror is used to see the same copy of the object. Likewise for the complex circuits duplicate current is generated from the current source. This generated current (I_{out}) fed into the circuit to reduce the complexity of the design. Current is drawn through the prime sender of current is termed as main current and copy of that main current (I_{ref}) is called replica of current or output current. Current mirror has the ability to scale up or scale down the reference current. For the complex circuit one reference current source is enough. To provide reference circuit to the other circuit in the design a specific arrangement is called a current mirror. Basically, a current mirror is a path in which current of the specific range is traveled one point to another end with same range [3]. Scaling up and scaling down of the current mirror is a very important issue. For this aspect ratio of the transistor has taken. To produce the double output current aspect ratio should be doubled for the current mirror. As we increase the aspect ratios current will increase or decrees according to it. High output impedance, low input impedance, speed, accuracy, and others are the main parameters of the current mirror. Lots of design for the current mirror like cascode CM, Wilson CM, modified Wilson CM, self-controlled CM, regulated CM etc. are utilized for these parameters. In general Transistor, stacking is used to enhance the resistance [4].But there are lots of techniques which can replace the stacking. Negative feedback, op-amps, current compensation and gain booster are used to increase the output impedance [4,5]. In this paper, basic configurations of the several CMs and the dual state op-amp are discussed. The experimental work is taking place on 32nm technology with the help of galaxy cdesigner in synopsis tool. Op-amps can also be used as a feedback element to enhance the gain and impedance of the current mirror. It is also called gain booster for current mirror [7]. In this paper, five sections have been discussed. Section I describe the introduction of current mirrors and give the insight of current mirror used. Section II shows the design of different types of current mirror topologies. Section III presents the presence of a current mirror in two stage op-amp. Section IV grants the experimental values obtained and section V mounts the conclusion.

II. ORGANIZATION OF CURRENT MIRRORS

2.1. Conventional Current Mirror

The current mirror is the two port device in which one port is the sender and another port is a receiver. Current is traveled through. One port to another end. An essential method of a CM imperializes basic two P-type MOS transistor M1 and M0. In the basic design of the current mirror, gate of the M1 is joined with the drain of the same transistor called diode connection. It means that this transistor will always in saturation mode. Figure 1 illustrates the traditional CM composition. The connection between gate and drain are formed diode connection termed as a diode-connected transistor. In the representation of traditional current mirror, V_{dd} is connected to the current source (I_s). The current source is further connected with the transistor M1 (diode-connected).When current from the current source (I_s) enters in M1 then M0 will be associated with same V_{gs} having the same current at the drain end of the transistor M0.Gate –source voltage of transistor M1 and M0 are same which helps to track the same current on the output side. Output current which is obtained from the reference current source depends on the aspect ratio of the two transistors [1,2].

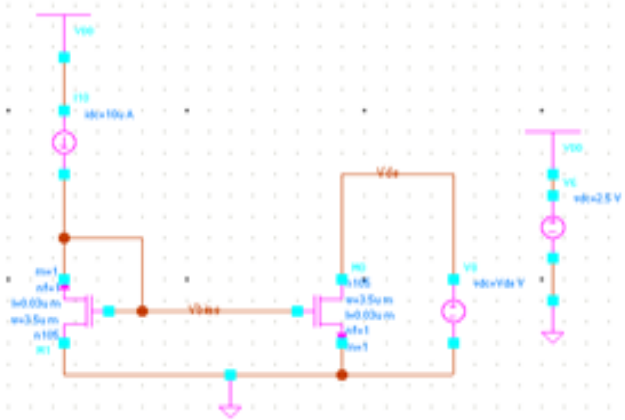

Figure 1.CMOS Implementation of Simple Current Mirror [1]

Suppose there is no channel length modulation then,

$$I_{ref} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1(V_{gs1}-V_{th})^2 \qquad (a)$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2(V_{gs2}-V_{th})^2 \qquad (b)$$

On solving a and b we have following outcomes:

$$I_{out} = I_{ref}\left(\frac{W}{L}\right)_2 / \left(\frac{W}{L}\right)_1 \qquad (c)$$

Idealistic highlights of the CMs are:

1. Obtained current must be equal to the input current multiplied by desired current gain.
2. Obtained current would be unyoked of yield voltage. In other words, output impedance should be infinite.
3. The gain of the current mirror should be independent of input signal frequency [1].

Limitation:

1. Output current varies with the output voltage, which will be characterized by output resistance.
2. A minimum positive voltage is required to operate the current mirror in the saturation region.
3. Gain lapse also causes limitation in the current mirrors [2].

Figure 2 elude the simulation results run on the Synopsis cdesigner tool. This waveform depicts the output voltage to output current.

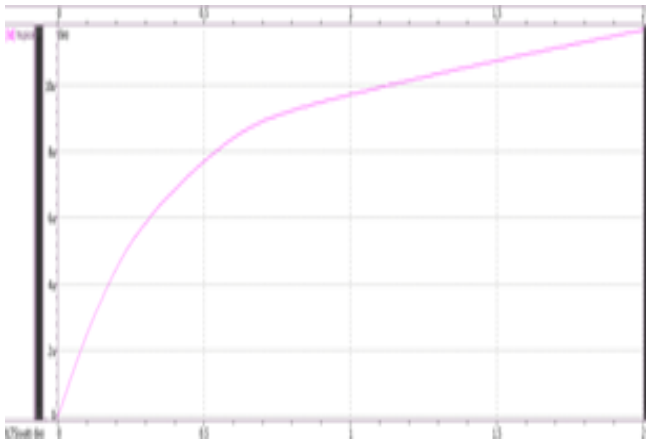

Figure 2. Basic Current Mirror Output Waveform

2.2. Cascode CM

A traditional CM has very low output impedance. So that to increase the impedance of the simple current mirror another transistor is added to the previous transistor. This transistor has separately V_{bias} element. Figure 4 depicts the cascode current mirror [9]. This is consists of four transistors. MN1 and MN2 are the diodes connected. The output transistor is MN4 where the output current is taken. In the conventional current mirror, the channel length modulation impact was not considered [8].

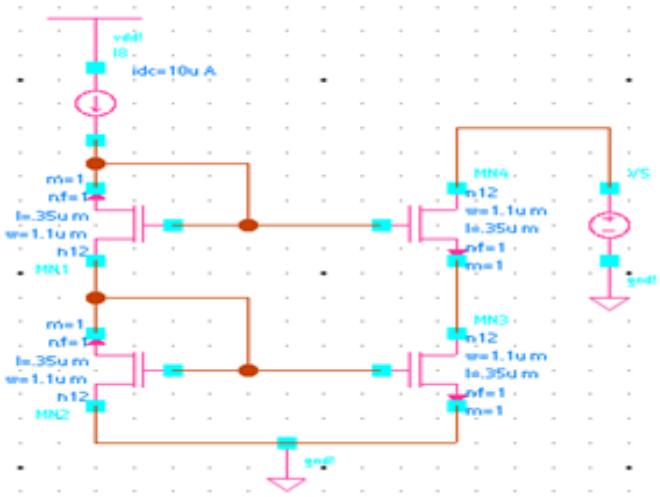

Figure 3. CMOS Implementation of Cascode Current Mirror [2]

This impact brings about the noteworthy mistake in duplicating current. In the case of the Simple current mirror drain–source voltage of the transistor is not equal. Therefore no same current is obtained at the drain end. The drain voltage of the transistor is affected by the extra circuit in the system.

Hence it is very necessary to make V_{ds1} equal to V_{ds2} with no channel length modulation.

A separate transistor MN4 is cascoded over MN3 to minimize the channel length modulation affect and impact of the drain to source voltage. MN4 is a separately biased transistor. V_{bias} is connected with the end goal that the voltage crosswise to drain –source of MN4 and MN3 will be equivalent. Along these lines, we can accomplish high yield resistance with the same replica of current I_{out} [9].

DC analysis has been accomplished in the synopsis galaxy c designer tool ate 32/28 nm technology. Below waveform in figure 4 demonstrate the output waveform of output current I_{out} to a voltage source.

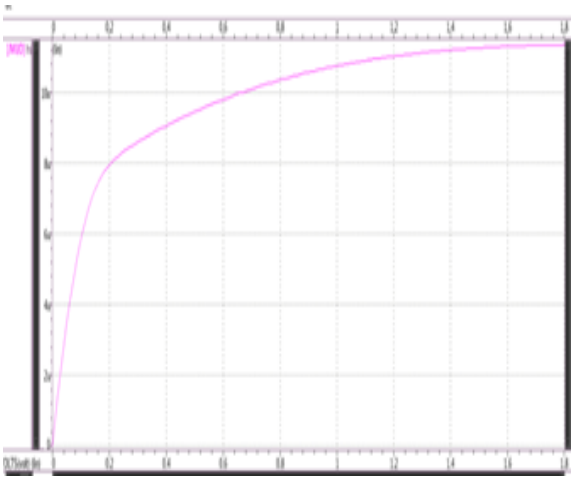

Figure 4.Cascode Mirror Output Waveform

2.3. Wilson CM

A Wilson CM is a circuit which anticipated an unfaltering current as showed up in figure 5.

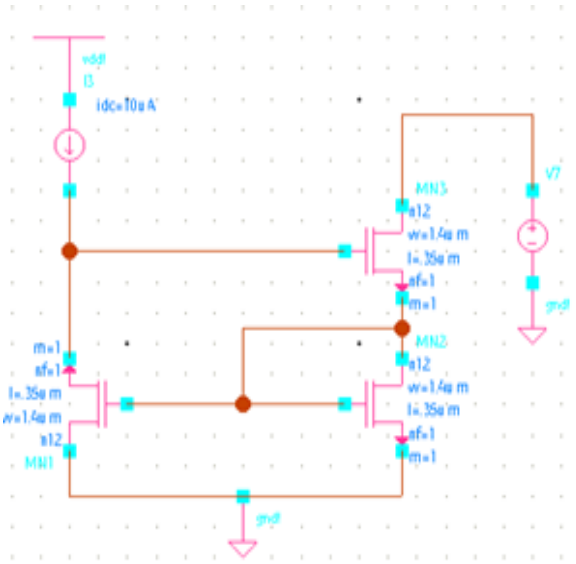

Figure 5. CMOS Implementation of Wilson Current Mirror [12]

A substitute idea is Wilson current mode, which utilizes negatory feedback praxis. As a result, this type of composition has been established to ensure the spacious obtained impedance [12]. Wilson CM is different from the other conventional mirror. It uses negative feedback and thus has advanced obtained impedance than other conventional CMs. The gate node of MN3 is associated to the point just above the MN1, which devises a steady reference voltage owing to the consistent current I_{ref}. Transistor MN2 is diode-connected; it remains in the saturation mode. To adjust the expansion in current through MN1, the voltage at point A drops and in this manner diminishing the entryway voltage of MN3. In this fashion general lessening in drain current of MN3 declines which balances obtained current [2].

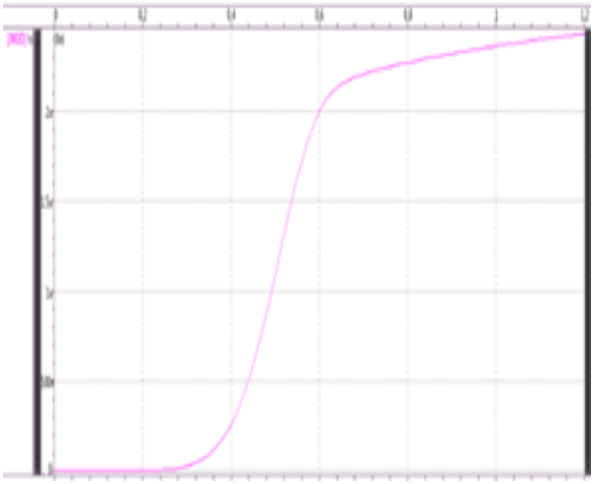

Figure 6. Output waveform of Wilson Current Mirror

Privative feedback is fed to this circuit using the plea that this texture will deliver chronic obtained current aimed at massive voltage blows and modified output impedance. In the construction of a traditional current mirror and cascode CM is not used feedback praxis.

2.4. Modified Wilson Current Mirror

In this design, it is comprised of four transistors as shown in figure 4.M1 is independently biased with V_{bias1}.V_{bias1} will be a biasing voltage which is utilized inclination the M1 transistor and V_{bias} is a settled voltage. So, when V_{bias1} is fixed I_{ref} is entering in M1 is consistent and also that current will course through M2. Transistor M3 is a diode-connected transistor and Transistor M4 is normal output transistor.

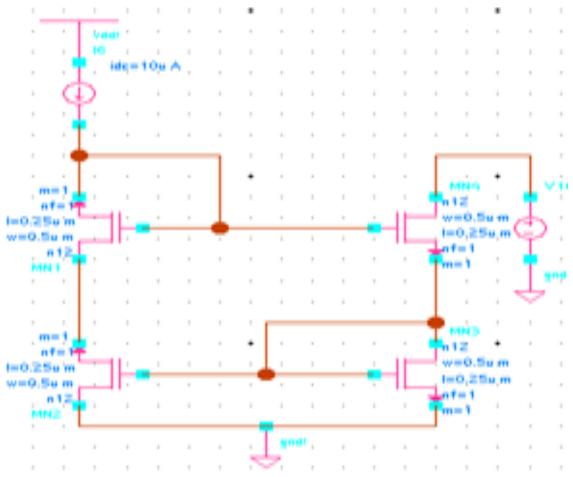

Figure 7. CMOS Implementation of Modified Wilson Current Mirror [12]

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Wilson current mirror will be having negative feedback in because of negative feedback drain current is settled and negative feedback is nothing but there are four distinct sorts of feedback are there [12]. Voltage series, voltage shunt, current series, and current shunt are the types of feedback.

In Wilson current mirror current series sampling is utilized. At whatever point sampling is utilized yield impedance will increment by (1+Aβ) [10].So yield impedance is more than the circuit which does not have any feedback.

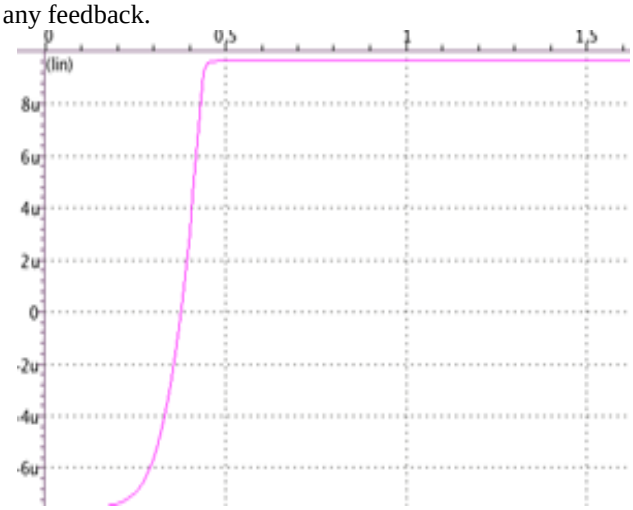


Figure 8. Output Waveform of Modified Wilson Current Mirror

For the modified Wilson current mirror flexion in the above graph is more. It has also a very good matching adroitness.

In Wilson current Mirror transistor M3 (figure 4) is diode connected however in regulated cascode transistor M3 is separate with an external voltage. Transistor M3 is diode-connected in Wilson current mirror is nothing but it is itself gives biasing. But when this connection is removed it needs to bias independently so that different V_{bias2} is used. The preferred standpoint of making this nothing but output impedance can be expanded by a large amount.

III. IMPLEMENTATION OF DUAL STATE OPERATIONAL AMPLIFIER

In the actual stage scenario execution of extraordinary signal processing and signal acclimatizing unit are an unconscionable role. In a large portion of the hardware circuits, the Operational Amplifiers is the most well-known building pieces. So as the transistor channel length and the power supply are lessened then the outline of Op-amps confront ceaseless test. Because of various aspect ratios (W/L), pact amongst rapidity, gain, power and other specification. By implementation of CMOS op-amps consolidate a significant DC gain with higher solidarity gain frequency has been a most factious issue. These two strategies can expand the gain, by expanding the yield resistance and input trans-conductance separately [13].

3.1. Design of Two-Stage Amplifier

Op-amp is the kind of the amplifier. An amplifier is anything we put on electronic signal in and get a larger version of the signal. Op-amp must have very high input impedance, very high open loop gain and very low output impedance. It is not possible to achieve in a single stage. This is why op-amp has three different stages. The first stage is differential amplifier. In this stage op-amp contains differential input. it has also high input impedance. It also enables user to utilize ideal op-amp equation for the circuit analysis. It also provides DC gain. The second stage is considered as gain stage. In this portion of op-amp it is responsible for the gaining up of the input and sending it to output stage. Finally, third stage is output stage. Op-amp must have low output impedance. This minimizes loading the output of the op-amp.

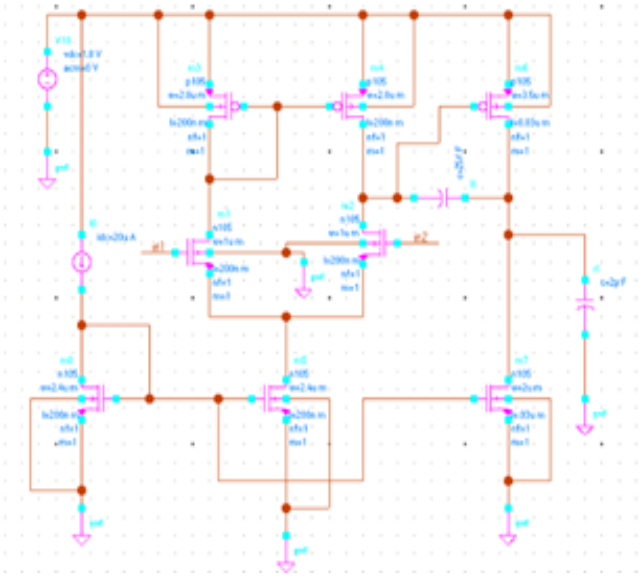


Figure 2. CMOS Implementation of Dual-Stage op-amp [2]

The purposed op-amp is consists of eight transistors. There are 3 N-type MOS and 5 P-type MOS transistors. This design of op-amp is divided into four parts. The N-type MOS M3 and M4 form the active load and P-type MOS M1 and M2 form Input for the op-amp. To increase the gain extra stage is also added to it. M8 and M5 forms current mirror. It gives bias current to op-amps. As this operation amp is composed on 32/28nm innovation scaling of the transistor likewise incites short channel impacts. The outcome of scaling additionally gives a few benefits and upgrades like less power consumption, enhance execution, ease, profitability challenges and so on. Experimental setup for the dual state operational amplifier has worked on the voltage range 0.8-1.2v. . To simulate this circuit we have used synopsis 64bit tool. Various parameters are obtained from the analyzer under SAE. Gain and phase margin are 78.6 and 68.8^{o} respectively configure from the analysis and shown in the figure.

Table 1. Aspect Ratio of Two-Stage Op-Amp

Transistor	Aspect Ratio (W/L)
M1,M2	4
M3,M4	14
M5,M8	12
M6	112
M7	25

As we have discussed earlier we have worked on the already existing two stage operational amplifier. For this amplifier we have used 32/28nm CMOS process.

Aspect ratio has huge effect on the circuit performance. Keeping this in mind we did analysis and find out appropriate aspect ratio for 32/28nm technology.

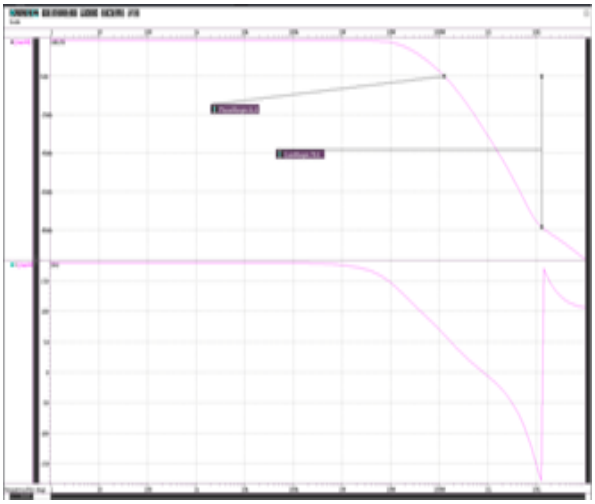
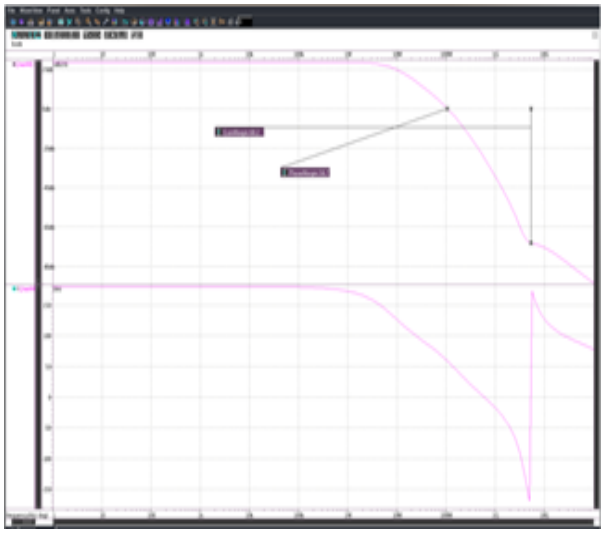


Figure 3. Results of the analysis came out to be is gain margin 78.6 db and phase margin 68.8^{o} degree



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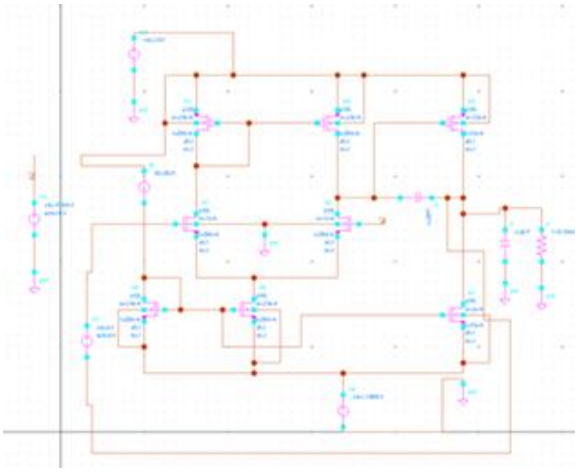

Figure 8. Design of Two-Stage op-amp for timing analysis

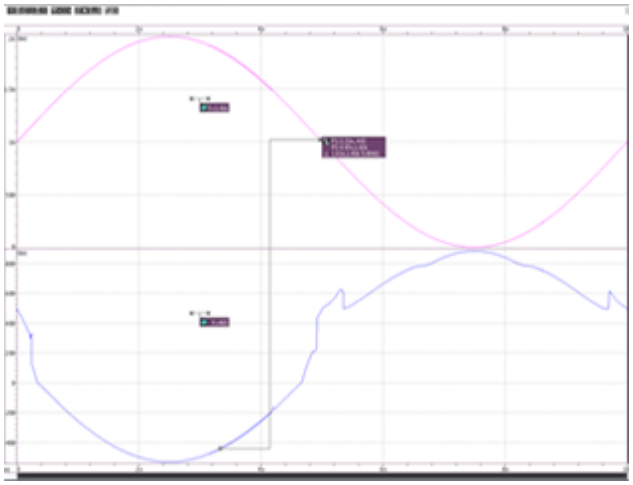

Figure 8.Output Waveform of Slew Rate for Op-Amp

The amplifier has the maximum rate at which output voltage can change known as slew rate. It is defined the maximum rate at which output voltage can change with respect to the input signal [13].

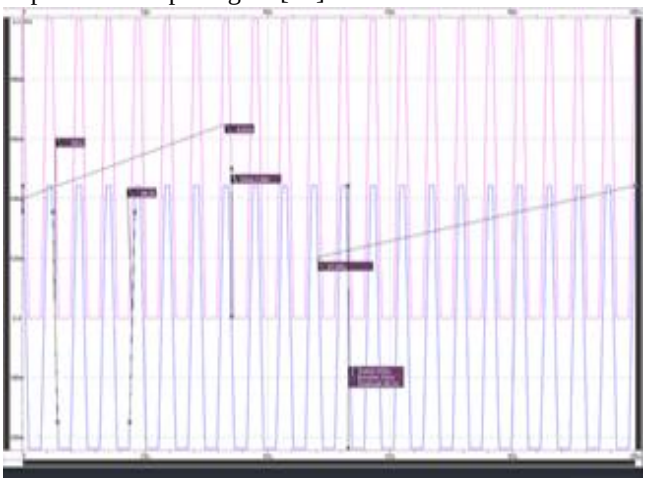

Figure 8. Output Waveform of Delay for op-amp

This is measuring by applying step function to the input. Slew rate determines how fast an operational amplifier responds to the input signal. In ideal case, operational amplifier output voltage will appear at the output node at the same instant when we apply the input voltage signal. But in the reality output voltage appear at the output terminal after same time period [10].

IV. SIMULATION RESULT

In this, we have worked on the 32/28nm process using galaxy cdesigner in synopsis red hat 64-bit. We have worked on already design two-stage amplifiers. In our purposed work, we have worked on the aspect ratio for 32/28nm process and got significant results.

4.1. Results and Discussion:

Considering the 32/28nm technology circuit is simulated on Synopsis galaxy cdesigner tool. The outcomes of this simulated circuit are compared with the circuit in [10]. The purposed circuit has huge gain with reduced channel length. All important parameters are drawn in table 2.

Table 2.Comparison Consequences Different Purposed Circuits

Factors	Basic CM	Cascode CM	Wilson CM	modified Wilson CM
V_{omin} (V)	0.2-0.5	0.4-.0.8	0.4-1.2	0.59-0.69
Input Resistance (Ω)	7.5K	8.23K	9.17K	3.9K
Output Resistance (Ω)	512K	6.5M	21M	37M
Power consumption (µW)	53.45	33.29	21.1	19.43
Stability	Poor	Good	Good	Better

In this work, the higher gain and phase margin of the two stage amplifier have presented.

4.2. Simulation Result of Various CMs Circuit:

The comparison result of parameters such as supply voltage, stability, output and input impedance, and power are given as follows.

Table 3.Comparison Results of various Current Mirror

Factors	**Technology**		
	180nm [10]	45nm [10]	32nm This work
V_{dd}(V)	1.8	1.8	1.2
Phase Margin	63.22°	60.92°	68.8°
Gain (db)	47.81	52.68	78.6

V. CONCLUSION

In this paper, Basic configuration of the current mirror has been purposed. Moreover, using simple current mirror two stage op-amps has been design at 32nm technology in synopsis tool. As current mirrors is the elementary part for the analog circuits. It provides biasing to the circuit and could be use as an active load. Additionally, ideal current mirrror has infinte impedance and zero input impedance. But generally it is not happen because of loading effect. Hence to minimize the loading effect it is very necessary that current mirror should have high output impedance and low input impedance. There are lots of techniques to enhance these factors like cascoded current mirror, regulated current mirror, resistor and capacitor compensation etc. Besides, In VLSI designing low power and low voltage is very important. Bulk driven, self-regulated, hybrid technique for the current mirror are used for low power circuits. Op-amps can also be used for the current compensation technique and to provide the feedback for the current mirrors. Further, to boost up the output impedance negative feedback has been introduced by Wilson and regulated current mirror. Moreover, to obtain maximum output impedance op-amp circuit can be used as a feedback.

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