Design of a Data Collection and Transmission System Based on AD9284

Tamkanath Sabeeha, Siva Yellampalli,

Abstract— this paper introduces a high speed dual channel data collection system based on AD9284 which can transmit data to PC by USB interface chip CYUSB3014. USB is more used than some traditional inter-PC Bus such as PCI due to the high speed and agility and also provides properly convenient communication interface for A/D conversion. This paper not only focusing on the characteristics of the AD9284, but also explains the interface circuit. By controlling the variation of the signal from analog to digital, the system achieves the point of the high-speed dual-channel data collection and real time monitoring, It can be primly used as a Spectrum analyzer or Oscilloscope in back-end receiver system.

Index Terms- AD9284; Data collection; PLL IC AD9510; USB3.0;

I. INTRODUCTION

An ADC is a critical component in a radio receiver design [1]. It is used to convert a continuous-time input voltage into discrete output levels which are represented by binary coded words. Advances in the development of ADCs, and the availability of increasingly faster and less expensive digital hardware are resulting in more of the traditional analog function of a radio receiver being replaced with digital hardware. This design chooses an ADC IC AD9284 from Analog devices has been selected for the design of High Speed ADC

Digitizer, which is a dual 8-bit, monolithic sampling ADC that supports simultaneous operation and is optimized for low cost, low power, and ease of use. Each ADC channel operates at up to 250 MSPS Conversion rate with outstanding dynamic performance, capable of digitizing full-scale voltage of 1V p-p input into 8-bit digital words with a power dissipation of about 314mW. In a small 48-lead LFCSP, it can meet the requirement of the small dual-channel data collection system.

In this design, USB3.0 is chosen as the transmission mode, USB3.0 has the advantages include easy installation, high bandwidth, super speed (480 Megabyte per second), low cost, high Stability and easy expanded, etc. [2]. This design picks up the CYUSB3014.

II. LITERATURE SURVEY

The trend in receiver design is evolving towards the goal of incorporating digitization closer and closer to the receiver antenna at increasingly higher frequencies and wider bandwidths. An intermediate frequency (IF) sampling receiver utilizes an ADC to sample the analog signal before it is converted to base band as shown in the Figure 1 However, there are many concerns that need to be addressed when sampling at higher carrier frequencies.

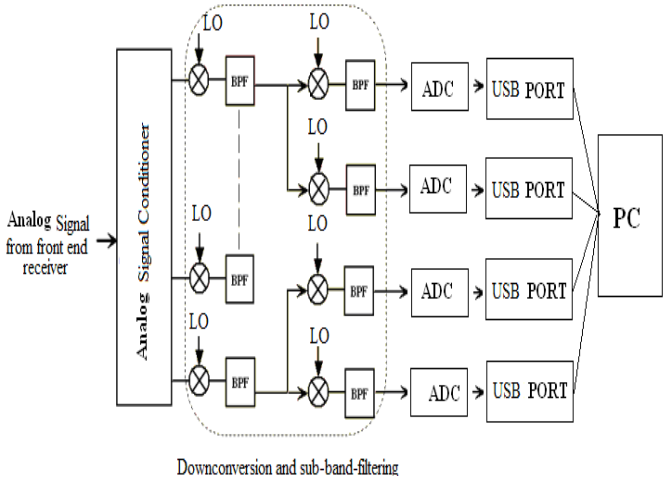

Figure 1 Block diagram of a high speed analog-to-digital converter in Receivers

The important concepts are aperture width and aperture jitter. The aperture width is the effective time duration over which the signal gets averaged to produce a given ADC output. The width of this window is inversely proportional to the Maximum input bandwidth that the ADC can accommodate. So, if a higher frequency carrier is input, then the ADC's averaging process will significantly degrade the strength of the sampled signal.

Aperture jitter or aperture uncertainty is the sample-to-sample variation in the encode process of an ADC which can be caused externally by jitter in the sampling clock, and internally by the sampling switch which does not open at precise times. Aperture jitter causes the ADC to sample at a different phase of the carrier wave than assumed which can lead to signal power loss and carrier phase measurement errors.

A. Choosing an ADC for Digitization

Some of the important specifications that need to be considered while choosing an ADC for broadband applications have been described [3]. The integration of ADC functionality into consumer equipment has been influencing the converter market with ADCs in many ways being treated like application specific integrated circuits. Apart from cost of the converter, there are a few key specifications of interest like: number of ADC bits (resolution), the analog input

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Tamkanath Sabeeha, Electronics and Communication, VTU/ VTU Extension Center, UTL Technologies Ltd, Bangalore, India.

Dr.Siva Yellampalli, Electronics and Communication, VTU/ VTU Extension Center, UTL Technologies Ltd, Bangalore, India.

bandwidth, signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR),

Signal-to-noise ratio and distortion (SINAD), power consumption and sample rate that can be used to select the right ADC for a given application [4].

These standards, ease of configuration, looking for plots showing the device performance as a function of analog input frequency, frequency of sampling clock, temperature and supply voltages, checking for specifications under the same condition in which the device is likely to be used, etc. Also, the Radio Frequency Interference (RFI) scenario in and around the operating frequency band needs to be taken into account in order to assess the linearity that can be provided by the ADC and estimate the actual number of ADC bits available for representing the signal of interest.

- *ADC Bit Resolution and Input Power*

A converter has a physical number of bits that usually corresponds to pins on the device. These are sometimes referred to as “marketing bits” or “resolution”. However, performance may or may not correspond to these physical bits. Typically, performance bits are fewer than the number of marketing bits. These bits are often called Effective Number of Bits (ENOB). To evaluate the number of bits necessary in an ADC system, the dynamic range of the input signal to the ADC has to be analyzed by carrying out a survey of the spectrum at the site where the radio telescope is likely to come up. Ideally, a radio telescope should receive only the sky noise and an 8-bit representation of the sky signal could be sufficient to describe it. But, due to the presence of stronger man-made RF signals (called RFI if they fall in a protected frequency band) increase in the received power has to be taken into consideration to avoid saturation of the converter.

- *Input Bandwidth*

In order to accurately sample high frequency signals, high analog bandwidths are required. Typically, in ADCs, the sampling mechanism is a capacitor and a switch. Converter bandwidth is largely determined by the value of the switch resister (R) and the sample capacitor (C). So, to maximize input bandwidth, both R and C should be minimized. But, wider input bandwidth allows more noise to pass the ADC input stages and be digitized, resulting in lower SNR than would be for a lower bandwidth ADC.

Therefore, for a given design, SNR is inversely proportional to bandwidth. This is one of the key reasons why high bandwidth converters have fewer SNR bits than the total resolution of the ADC. Conversely, wider input bandwidth allows for better slew-rate performance and more accurate tracking of the fast slewing analog signals associated with both transient events and high-frequency sine waves. It also allows wideband analog signals to be accurately sampled by the accompanying faster sampling rate.

While, for optimal spurious performance, a wide input bandwidth is desirable, the increased bandwidth with smaller C allows more noise to enter the front-end of the ADC and be spread across the Nyquist spectrum resulting in the degradation of SNR. Thus, SNR and SFDR must be traded for one another. Usually, the input bandwidth specification is representative of the flatness of the ADC response versus input frequency and is not an indication that the device will hold the performance up to those input frequencies.

Hence, it is important to note the manufacturer’s specifications for SNR, SFDR and ENOB for different input RF frequencies and sampling clocks, as these dynamic specifications of the ADC decreases at the higher frequencies because the effects of jitter get worse. The other issue that crops up with higher analog bandwidth is that of interfacing the analog input to the ADC. For higher Intermediate Frequencies (IFs) and direct RF sampling applications, proper impedance matching to the source becomes more critical. At high frequencies, optimal ADC performance is achieved when a proper match exists.

- *Power Dissipation*

Although usually not considered directly as a performance metric, power consumption does factor into most ADC figure-of-merit calculations, indicating that the lower the power, the better the figure-of-merit. While ADC power consumption is of serious concern in hand-held devices, it does affect the overall power budget of a receiver system. The thermal management of the ADC needs to be taken care of by providing a suitable heat-sink, maintaining the specified air-flow (if forced cooling is required), and constantly monitoring the converter’s temperature so that a suitable action can be taken if the device’s temperature exceed specified limits.

- *Sampling Rate*

Typically, a converter’s best performance is limited to the first two Nyquist zones, confining the input frequency of the ADC to being less than the maximum frequency of the sampling clock specified by the manufacturer. As the maximum frequency of the sampling clock for high-speed analog-to-digital converter increases, so does the width of the Nyquist zones. Additionally, for converters with a higher maximum sampling rate, the analog anti-aliasing filters have more room for transition from pass-band to suppression than for a lower sampling-rate device, thereby, easing the requirements of the filter

This brings up the possibility of connecting a high-speed ADC to a computer via USB Higher sampling rates improves noise performance of the ADCs. While the overall integrated noise does not improve, the distribution of the noise over wider bandwidth does offer improvements in noise spectral density (NSD). This process is often referred to as processing gain and is nothing more than distributing the same noise power over a wider band of frequencies.

III. GENERAL DESCRIPTION OF AD9284

A. Function

The AD9284 is a dual 8-bit, monolithic sampling,

analog-to-digital converter (ADC) and requires a single 1.8V supply and an encode clock for full performance operation. No external reference components are required. The digital outputs are Low voltage Differential Signaling (LVDS) compatible. Figure 2 show the internal functional block of AD9284 [5].

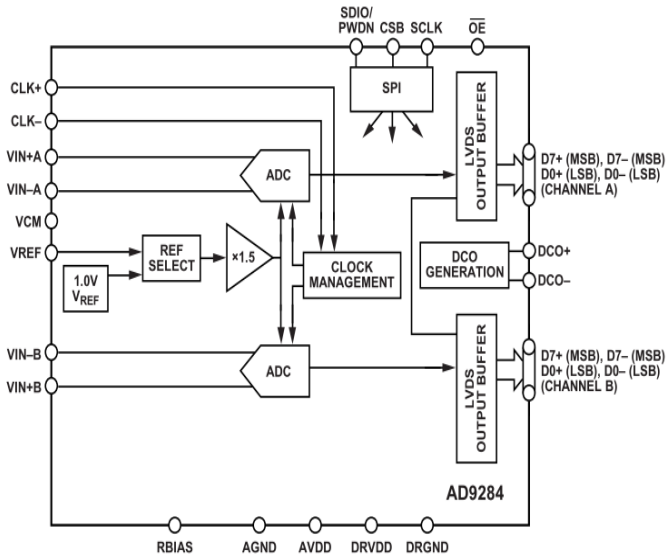

Figure 2 Internal functional block

Each channel of the AD9284 consists of a differential input buffer followed by a sample-and-hold amplifier (SHA). The SHA is followed by a pipeline switched-capacitor ADC. The quantized output from each stage is combined into a final 8-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, whereas the remaining stages operate on preceding samples.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor Digital to Analog Converter (DAC) and inter-stage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The input stage contains a differential SHA that can be ac-or-dc-coupled in differential or single-ended mode. The output staging block aligns the data, carries out error correction and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers enter a high impedance state [5].

B. Channel selection

Some channel setup functions can be programmed differently for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in the memory map register table as local. These local registers and bits can be accessed by setting the appropriate channel A (Bit 0) Or Channel B (Bit 1) bits in register 0X05.

If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. We choose Channel A here.

C. Starting the conversion and data reading

A typical AD9284's conversion timing sequence is shown in Figure 3.

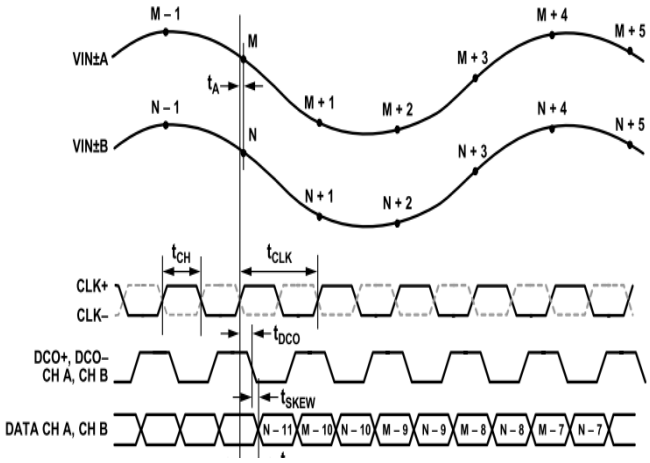

Figure 3 Timing Sequence

IV. DESIGN OF HARDWARE

Figure 4 shows the general frame of the system. The input and output of the ADC IC AD9284 is in Low Voltage Differential Signaling (LVDS) form. Therefore the analog signal should be first given to the analog filters outside the board and through right angled SMA connector the analog signal is first given to the differential amplifier IC ADA4937-2 which converts the single-ended to Differential signal. These differential analog signals are then given to the ADC IC AD9284 which samples the signal at the sampling rate of 250MSPS. And gives the LVDS output which is then given to the USB3.0 chip CYUSB3014 for data acquisition and interface to the PC or Laptop.

One of the important constraints in this design is that, the power supply required for the board is taken from the USB connector as shown in the Figure 3, here the 5 Volts from the VBUS pin of the USB3.0 connector is given to the DC-DC converter ADP5034 which is a multi-output regulator and converts the 5V to 3.3V, 2.5V, 1.8V and 1.2V dc voltages required for different AD9284 IC and CYUSB3014 IC.

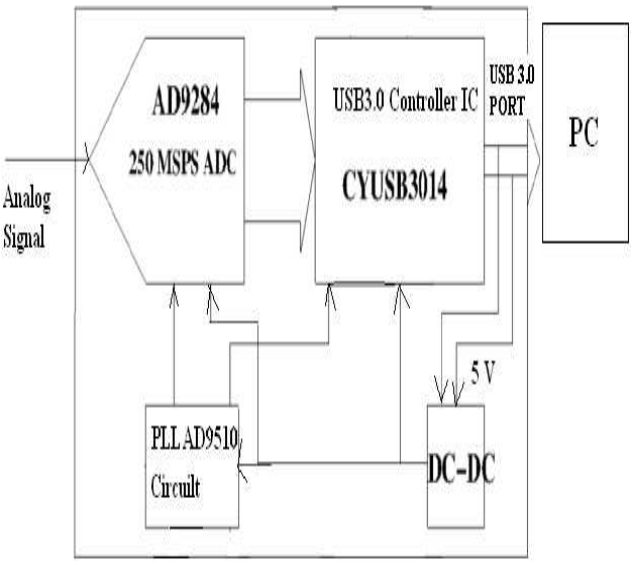

Figure 4 System Frame

A. Interface hardware design of AD9284 and PLL circuit

Before entering into the ADC the signal has been processed by the active low-pass second order filter, it is standard process. The design uses onboard PLL circuit for supplying sampling clock to the ADC. To meet the PLL circuit requirement to generate a Clock of frequency 250MHz, PLL IC AD9510 from Analog devices has been selected for clock generation circuit. The AD9510 provides a multi-output clock distribution function along with an on-chip PLL core. The design emphasizes low jitter and phase noise to maximize data converter performance.

Figure 5 shows the typical link between PLL circuit and the AD9284. The PLL section consists of a programmable reference divider (R); a low noise phase frequency detector (PFD); a precision charge pump (CP); and a programmable feedback divider (N). By connecting an external VCO to the CLK2/CLK2B pins, frequencies up to 1.6 GHz can be synchronized to the input reference.

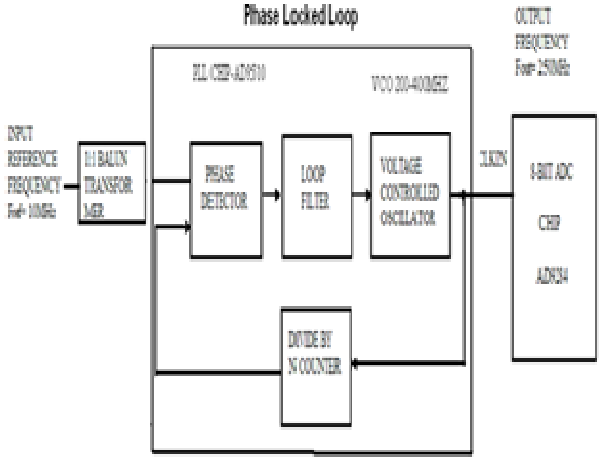

Figure 5 Interface circuit

There are eight independent clock outputs. Four outputs are LVPECL (1.2 GHz) and four are selectable as either LVDS (800MHz) or CMOS (250MHz) levels.

B. Interface design of AD9284 and CYUSB3014

- *General description of EZ-USB-FX3 (CYUSB3014)*

CYUSB3014 USB 3.0 is the next generation USB 3.0 peripheral controller providing highly integrated and flexible features. It has a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. It provides easy and glue less connectivity to popular interfaces such as asynchronous SRAM; asynchronous and synchronous Address Data multiplexed interface and so on [2]. The interface design of AD9284 and CYUSB3014 is shown in Figure 6. The maximum input voltage on USB3.0 controller IC CYUSB3014's VBUS pin is 5V .in this case, it is necessary to have an external Over Voltage Protection (OVP) device to protect CYUSB3014 USB3.0 controller IC from damage on VBUS.

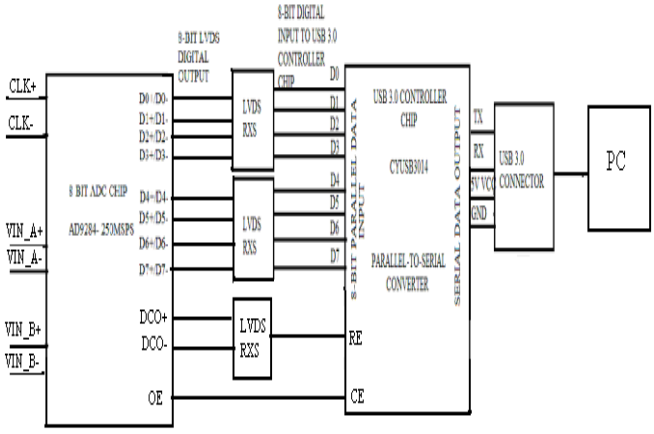

Figure 6 interface design of AD9284 and CYUSB3014

USB3.0 controller IC has built-in- ESD protection on the D+, D-, GND pins on the USB interface. The ESD protection levels provided on these ports are:

1. +/- 2.2 KV Human Body Model (HBM) based on JESD22-A114 Specification.
2. +/- 6 KV Contact Discharge and +/- 8 KV Air Gap Discharge based on IEC61000-4-2 level 3A.

This protection ensures the device will continue to function after ESD events up to the levels stated.

- *Interface hardware design*

The interface mode of EZ-USB FX3 includes modes as Slave FIFO and GPIF II (general programmable interface II) mode. This paper adopts GPIF II mode.

The GPIF II interface is configured by creating a GPIF II state machine. 8 kB of memory space is allocated to store GPIF II state machine definition.

Each state is defined by 32 bytes in (SRAM) memory. These 32 bytes define the properties of a state and the trigger conditions that can cause state (or I/O) transitions. Each state has two transitions out of it.

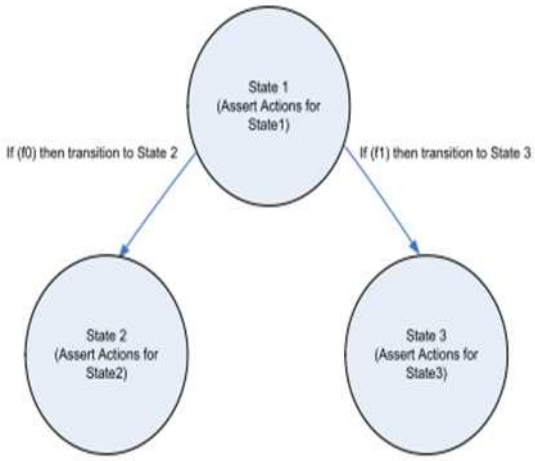

Figure 7 GPIF II state transitions

The transition out of a state is determined based on transition conditions. The transition is associated with both external and internal triggers. Each state is programmed to perform certain actions. The transition conditions are checked on each GPIF II clock edge or after a programmable number of clock cycles. Figure 7 is a simple depiction of the basic structure of a GPIF II state

- f0 and f1 are logical functions of triggers.
- f0 is checked first. If f0=true, then GPIF II transitions from State 1 to State 2.If f0 = false, then f1 is checked.
- If f1= true, then GPIF II transitions from State 1 to State 3.
- If both f0 and f1 evaluate to false, then GPIF II remains in State 1. At the next clock, the conditions are checked again.

In Figure 8, the three GPIF II states are IDLE, READ and WRITE.

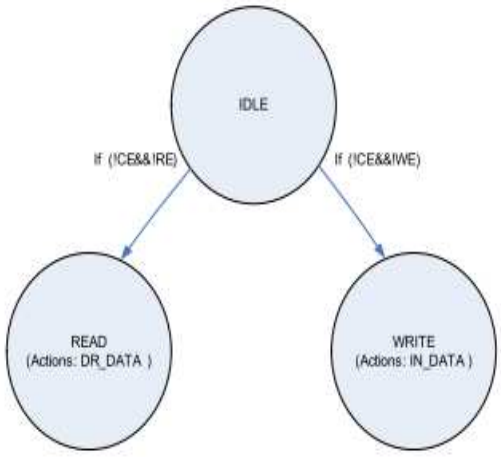

Figure 8 GPIG II State transitions with Actions

V. SOFTWARE PROGRAMMING OF DESIGN

The software programming design mainly consists of the AD9284's data collection block and the data transmission block via CYUSB3014. The programming language is C++.

A. Programming of data collection

On the basis of the AD9284's property and timing sequence, the control program of the data collection block decides to use the idea of "state machine". As is shown in figure 6, there are 3 states in the program, IDLE, READ and WRITE. No actions are asserted in the IDLE State. The CE (chip enable), RE (read enable) and WE (write Enable) signals are the trigger signals. These are the control input signals to GPIF II and are driven by an AD9284 device. The transition conditions are formed with these signals. The left transition condition is (! CE&&RE) (a read operation) and the right transition condition is (! CE&&WE) (a write operation). If the left transition condition evaluates to true, then GPIF II transitions from the IDLE state to the READ state. If the left transition condition evaluates to false, then the right transition condition is checked. If the right transition condition evaluates true, then GPIF II transitions from IDLE to WRITE state. If neither left nor right conditions evaluate to true, then GPIF II remains in IDLE.

B. Programming of data transmission

USB firmware

- USB firmware is a code which runs in the USB3.0 controller FX3 chip CYUSB3014, when the USB device connects to the computer; we generally take the following two methods to download the USB firmware to the RAM of FX3. Firstly, to make the firmware saved in the EEPROM out of the chip and gets the electricity to make the firmware loading automatically.

- Secondly, to design a device driver program which can finish the firmware loading automatically and realize the function of multiple enumerations named firmware download driver program.

- In this part of design, data are unidirectional transmission to PC, so we only need to program the "write operation". In the CYUSB3014, there are two "write operation", synchronous write operation and

Asynchronous write operation. We choose the latter here. Same with the program of data collection block we still pick up the idea of "state machine".

Cypress Corporation provides a complete structure or firmware program and allows users to develop under the environment of KEILC51 in order to simplify and accelerate the process of USB peripherals developing by EZ-USB FX3 chip for users.

So we just need to provide a USB descriptor's table and add the communication code of receiving and sending data for other endpoint as shown in Figure 9 and Figure 10.

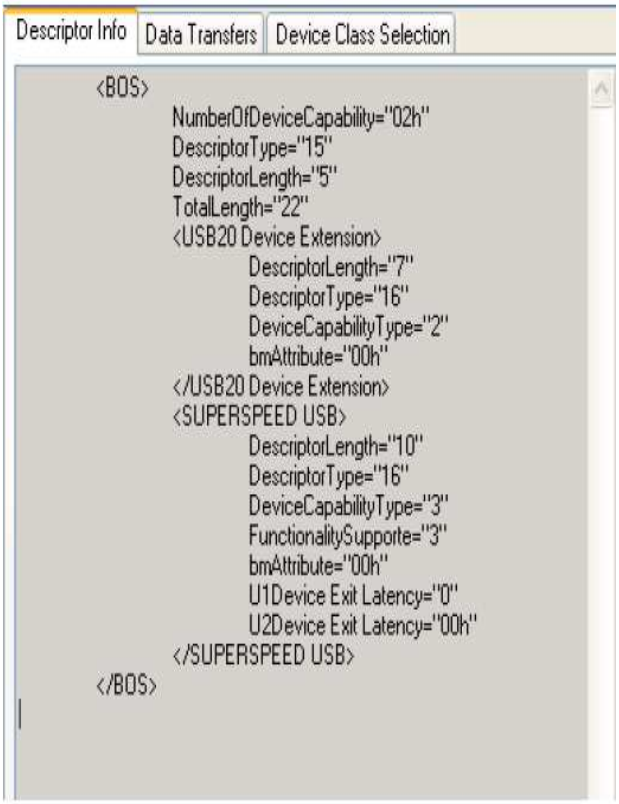

Figure 9 Snap shot of USB BOS Descriptor

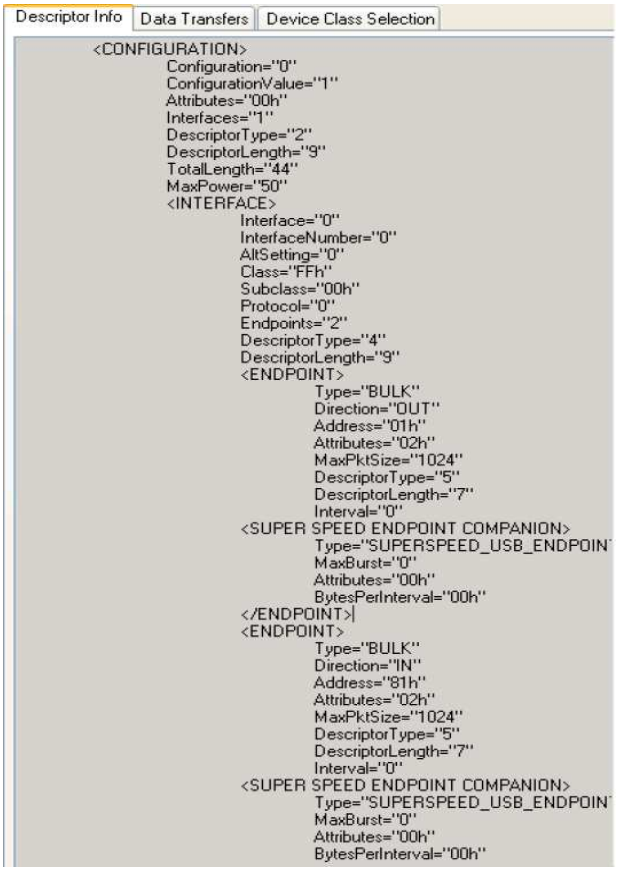

Figure 10 Snap shot of USB Configuration

Device action

Reconnect device button power-cycles the USB port to which a CYUSB3014 chip is attached. Power-cycling a port causes the device to be removed and re-enumerated.

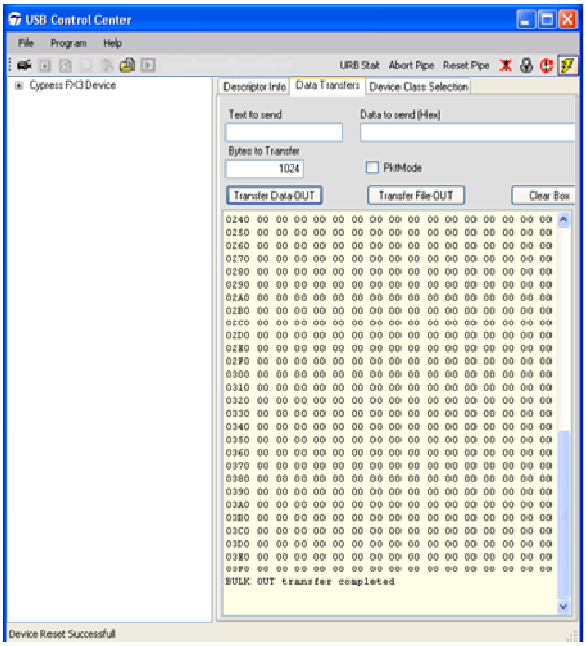

Figure 11 Snap shot of Device Reset action

Reset button reset the USB upstream port that is associated with the CYUSB3014.

After a successful reset as shown in Figure 11the bus driver re-selects the configuration and any alternative interface settings that the device had before the reset occurred. All pipe handles, configuration handles and interface handles remain valid.

Data transfer

Steps to Control Transfer

1. Select the control endpoint using the device tree view.
2. Indicate whether the data is to be sent to the device OUT or read from the device IN using the direction Combo box.
3. Indicate the type of request
4. Indicate the target.
5. If the direction is OUT fill the bytes to transfer field with the size of data expected from device and initiate the transfer using Transfer data button. The bulk out transfer data completed is shown in Figure 12.

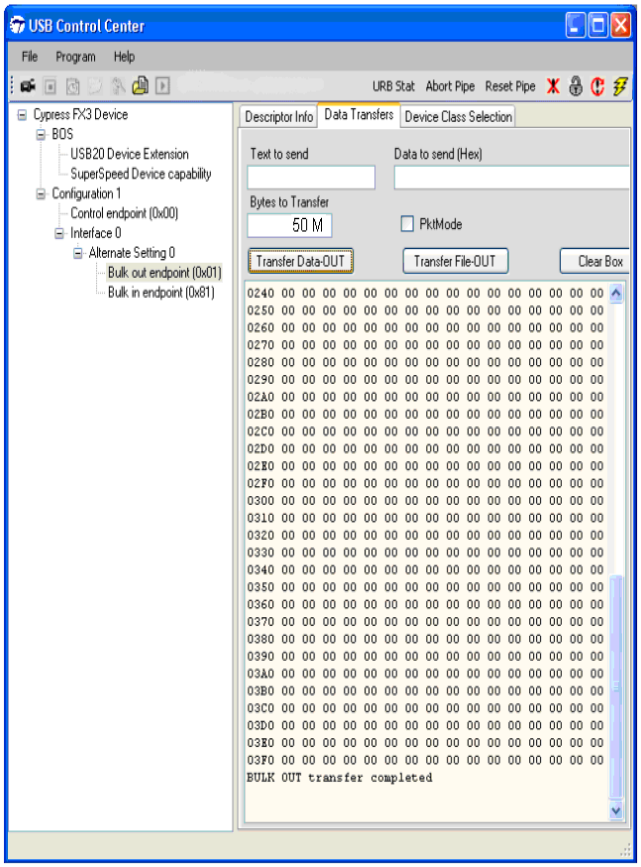

Figure 12 Snap shot shows BULK OUT transfer completed

Software programming

VI. PROGRAM SIMULATION AND TESTRESULT OF THE AD9284 USING VISUAL ANALOG TOOL

1. Connect and power the AD9284 digitizer board with FX3- CYUSB3014 USB3.0 port interface for data transfer. Also supply sampling clock of 250 MHz and input signal 1Vp-p, 10MHz to the AD9284.

Figure 13 Snap shot of driver installation dialog

2. Connect the FX3-CYUSB3014 USB3.0 interface port to the Laptop or Computer with a high speed USB cable. A driver installation dialog appears as shown in Figure 13.

3. Start Visual Analog,

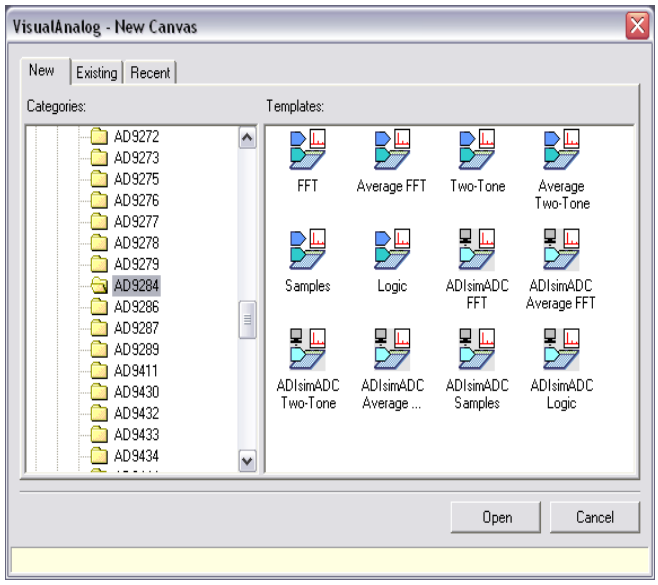

Figure 14 Snap shot of Canvas template that supports the ADC on the start-up form

Visual Analog attempts to detect ADC device and selects the Canvas template that supports the ADC on the start-up form as shown in Figure 14.

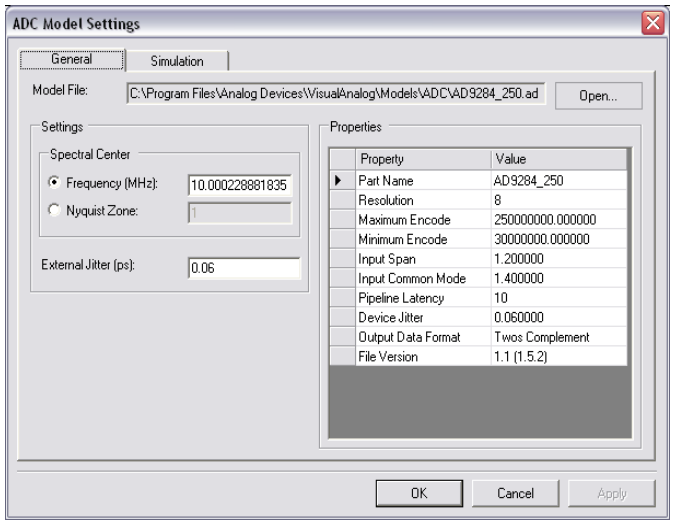

Figure 15 Snap shot of ADC model file

4. Set the Sample Frequency (MHz) to 250. Also, change the Samples text to 16384, by entering the text manually. Update the Use Composite Amplitude (dB) to -1 to evaluate ADC performance.

5. In ADC model, click the Settings…button and click Open to browse for and select the AD9284_250.adc model file as shown in Figure 15.

6. In Input Formatter click the settings… button then change the Number Format to two's Complement. Next, change both the Resolution and Alignment to 8. Click OK as shown in Figure 16.

7. There are two wires connected to the graph to route ADC samples as well as the FFT results. To see the time domain

representation of the data, click the Toggle Additional Plot button view the second plot.

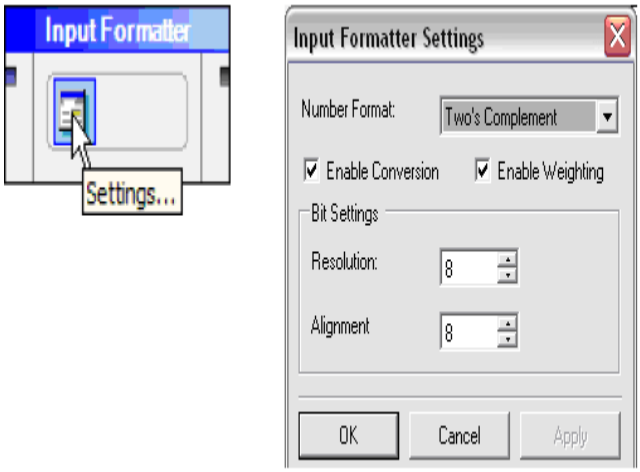

Figure 16 Input Formatter Settings

8. After making all required adjustments, update the **Canvas**. There are three ways to update the canvas, Select the menu command **Canvas**, and click **Update** or **Canvas**, and select **Continuous Update.** The Snap shots of the Outputs obtained are shown in Figure17 and Figure 18.

9. For analog input signal with frequency 0.5 MHz, the output obtained is shown Figure 17. And the values of SNR and SFDR are obtained as follows.

SNR= 48.348 dB, SFDR= 64.646 dBc and the harmonic powers obtained are

Harm 2 Power= -74.158 dBc.
Harm 3 Power= -64.646 dBc.
Harm 4 Power= -79.031 dBc.
Harm 5 Power= -72.301 dBc.
Harm 6 Power= -79.031 dBc.

10. For analog input signal with frequency 15 MHz, the output obtained are shown in Figure18. And the values of SNR and SFDR are obtained as follows.

SNR= 48.307 dB, SFDR= 64.562 dBc and the harmonic powers obtained are

Harm 2 Power= -70.049 dBc.
Harm 3 Power= -64.562 dBc.
Harm 4 Power= -78.99 dBc.
Harm 5 Power= -70.377 dBc.
Harm 6 Power= -78.99 dBc.

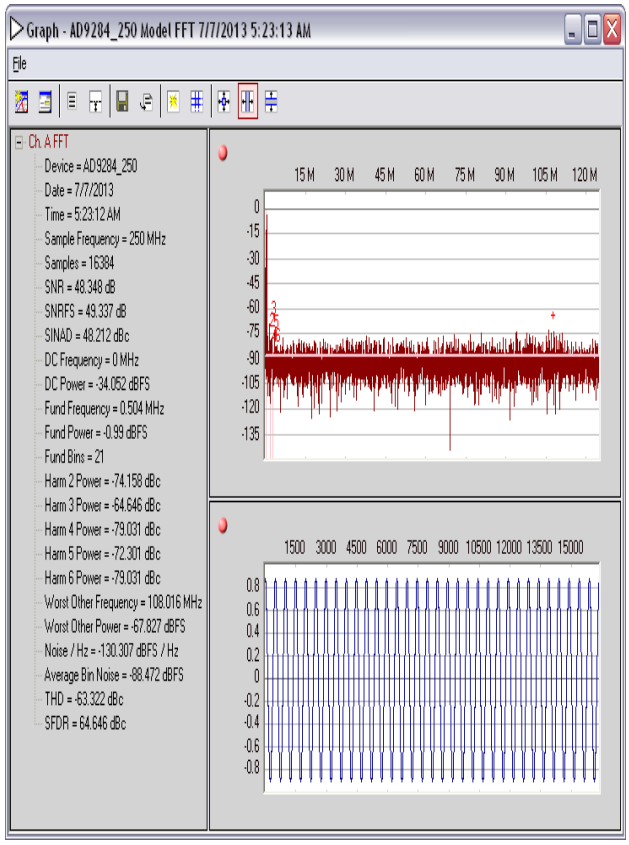

Figure 17 Output Result for Input= 1V, 0.5MHz and sample frequency= 250MHz

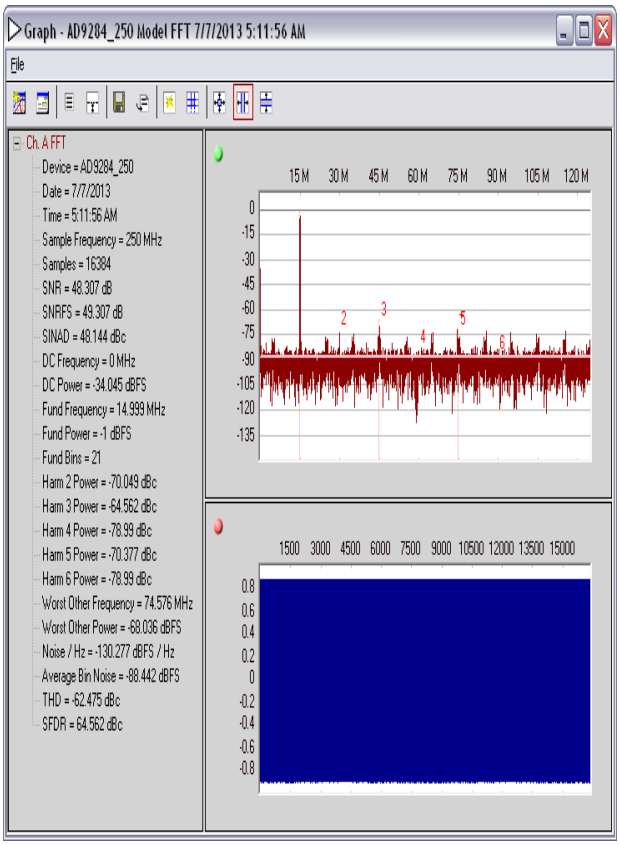

Figure 18 Output Result for Input= 1V, 15MHz and sample frequency= 250MHz

11. For analog input signal with frequency 200 MHz, this does not satisfy the Nyquist Criteria which says that for the

proper sampling the sample frequency should be equal to or greater than input frequency. The output obtained is shown in Figure 19 and can observe the Aliasing effect in the result. The values of SNR and SFDR are obtained as follows

SNR= 48.342 dB, SFDR= 0.001 dBc and the harmonic powers obtained are

Harm 2 Power= -70.216 dBc.
Harm 3 Power= -69.684 dBc.
Harm 4 Power= -0.001 dBc.
Harm 5 Power= -32.789 dBc.
Harm 6 Power= -0.001 dBc.

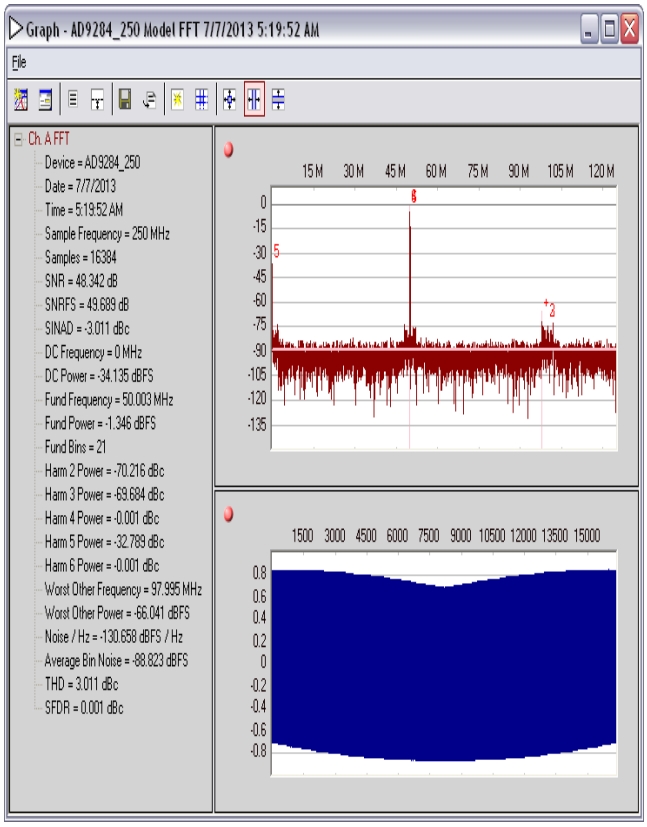

Figure 19 Output Result for Input= 1V, 200MHz and sample frequency= 250MHz

VII. CONCLUSION

In this work we have introduced the property of AD9284 and the application in data collection. Describe the design method of data collection system consisted of Ad9284 and CYUSB3014. Meanwhile, it gives the test results by this system which is well applied in the test of back-end radio receiver to analyze the Spectrum of the Cosmic rays.

The scheme introduced by this passage breaks in instances of data collection and transfers of large data and high speed. Compared with other schemes: this one owns many features such as small volume, low power dissipation, lower coat and so on. It simplifies the design of external hardware and improves stability and reliability of the system. The scheme has been implemented high and credible communication between the embedded system and PC through USB.

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Tamkanath Sabeeha. Was born in Mysore, India. She has graduated in Electronics and Communication Engineering in 2005 from VisveswarayaTechnologicalUniversity, Bangalore, India. Currently she is doing and her M.Tech in VLSI Design and Embedded System from Visveswaraya technological University. Her main research interest is Analog Communication and embedded Systems.

Dr. Siva Yellampalli is currently working as a Professor with VTU Extension Centre, UTL Technologies Ltd. He obtained his MS & Ph.D. from Louisiana State University. His area of research is system level design for power optimization. His area of research encompasses different research fields such as Very Large Scale Integration (VLSI), mixed signal circuits/systems development, micro-electromechanical systems (MEMS), and integrated carbon nanotube based sensors. He has published a book in the area of mixed signal design, and edited two books on carbon Nano tubes. He also published multiple International Journal papers & IEEE Conference papers in these areas of research.