Optimization of Geometrical Parameters of Gate-all-around Tunnel FET for Analog RF Applications

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Abstract--This paper presents the gate oxide thickness, gate oxide material, gate material and gate contact alignment variation impact on on-current, off-current, subthreshold swing, RF and stability performance of Gate-all-around Tunnel FET. The RF figures of Merit (FoM) such as cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) along with Stability factor (K) and dc parameters are calculated for different gate oxide thickness, gate oxide material, gate material and gate contact alignment. One parameter is varied at a time to show the resulting fluctuations in the device characteristics. The process variations show significant changes in the device performance and provide information about acceptable variations and design guidelines for GAA-TFET.

Keywords-- Gate-all-around Tunnel FET, Band-to-band Tunneling, Radio Frequency (RF), Technology Computer Aided Design (TCAD).

I. INTRODUCTION

Reducing the power consumption is the key to a new generation of energy-efficient electronics. The down-scaling of the operating voltage V_{dd} can significantly reduce the power consumption. However, to ensure reliable functionality, a minimal ratio of I_{on}/I_{off} is necessary, but the minimal inverse subthreshold slope of S = 60 mV/dec at room temperature limits the scaling of V_{dd} for a desired on/off ratio. Tunnel FETs have raised a lot of interest recently [1-6] because of their potential to allow S < 60 mV/dec at very low V_{dd} due to field-effect controlled band-to-band tunneling. When the device is turned on, the carriers tunnel through the barrier for current to flow from source to drain. When the device is off, the barrier keeps the off-current extremely low. In a gate-all-around structure the on-current is improved, while the off-current is furthermore lowered. This paper describes the design, dc characteristics, stability and RF behaviour of GAA TFET for various parameter variations like gate oxide thickness, gate oxide material, gate material and gate contact alignment. The simulations are performed using technology computer aided design (TCAD) tool.

II. DEVICE STRUCTURE AND SIMULATION

The structure considered here is a Gate-All-Around Tunnel FET with gate length (L_g) 10nm and gate oxide thickness (t_{ox}) 1nm. The device is uniformly doped at the source region, intrinsic channel region and drain region with concentrations 1×10^{20} cm^{-3}, 1×10^{17} cm^{-3} and 1×10^{20} cm^{-3} respectively. A non-local band to band tunnelling model is used along with Fermi-dirac statistics and Shockley-Read-Hall recombination model for simulation in ATLAS.

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The threshold voltage (V_t), sub-threshold swing, off-current (i_{off}) and maximum on-current (i_{dsmax}) are extracted from the dc characteristics and found to be 0.134 V, 54.27 mV/decade, 5.89×10^{-11} A/µm and 1.28×10^{-5} A/µm respectively. RF and small-signal ac analysis is performed to obtain the intrinsic and extrinsic parameters of GAA TFET from which f_t and f_{max} are calculated. Stability analysis is also performed and found that the device is unconditionally stable from 32.8GHz onwards. These parameters f_t, f_{max} and stability factor (K) are used to evaluate the high frequency performance of the device. Fig 2.1 shows the Gate-all-around tunnel FET structure.

III. IMPACT OF PARAMETER VARIATION

The impact on on-current, off-current, subthreshold swing, RF performance and stability due to changes in gate oxide thickness, gate oxide material, gate material and gate contact alignment are studied and presented in this section.

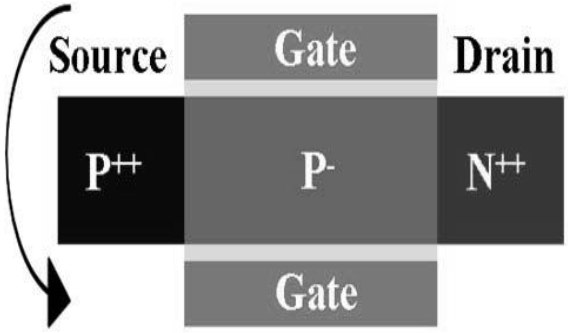

Fig.2.1 Gate-all-around Tunnel FET structure

A. Impact of Gate Oxide

1) Gate Oxide Thickness Variation

The gate oxide provides capacitive coupling between the gate and the channel which controls the drain current of GAA-TFET. Thus in short channel devices, the impact of gate oxide thickness on device performance cannot be ignored. The gate oxide thickness variation (Δt_{ox}) causes fluctuation in GAA-TFET dc characteristics, RF and stability performance.

The subthreshold swing is found to reduce with the increase in oxide thickness. Fig 3.1 shows the variation in subthreshold swing for various values of oxide thickness. The off-current also reduces considerably with the increase in oxide thickness, which is shown in Fig 3.2. The above two variations are advantageous with respect to GAA-TFET operation. Whereas the on-current reduces for $\Delta t_{ox}=\pm0.5$nm which is not desirable. The on-current variations are shown in Fig 3.3. Gate oxide thickness variation has no impact on the stability performance. Fig 3.4 shows the impact on f_t and f_{max}. Both the parameters show slight reduction for $\Delta t_{ox}=\pm0.5$nm.

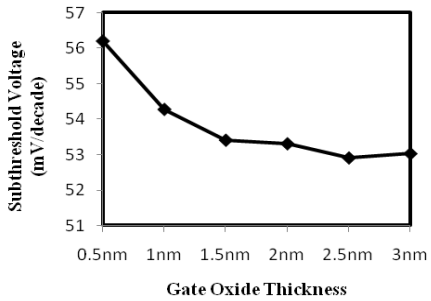

Fig.3.1 Impact of Gate Oxide Thickness Variation on Subthreshold Swing

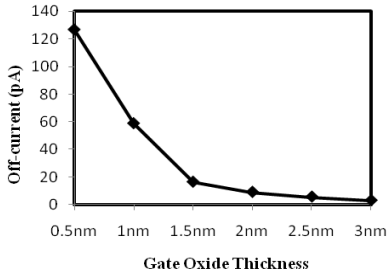

Fig.3.2 Impact of Gate Oxide Thickness Variation on Off-current

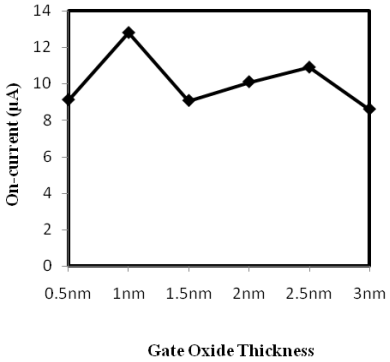

Fig.3.3 Impact of Gate Oxide Thickness Variation on On-current

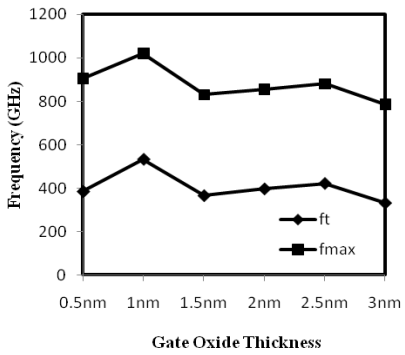

Fig.3.4 Impact of Oxide Thickness Variation on f_t and f_{max}

2) Gate Oxide Material Variation

The characteristics of gate-all-around tunnel FET for various gate oxide materials like Al_2O_3, ZrO_2, Ta_2O_5, La_2O_3 and HfO_2 are studied. The potential barrier found in tunnel FETs due to the presence of gate dielectric, influences the electrical characteristics, notably the I_{on}. The best performance is achieved by the device with HfO_2 dielectric. Higher on-current and improved f_t and f_{max} are obtained with HfO_2 dielectric. Fig 3.5 shows the impact on I_{on} for various gate oxide materials. The improvement in f_t and f_{max} can be seen in Fig 3.6.

The impact on the frequency at which the stability factor K=1, can be visualised in Fig 3.7.

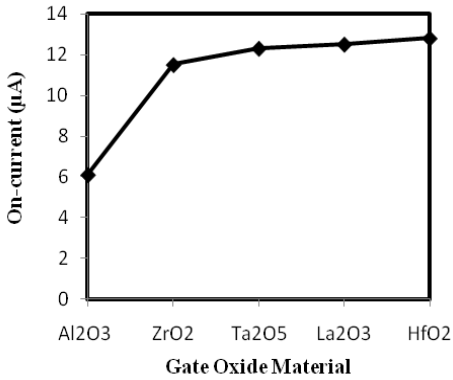

Fig.3.5 Impact on I_{on} for various Gate Oxide Materials

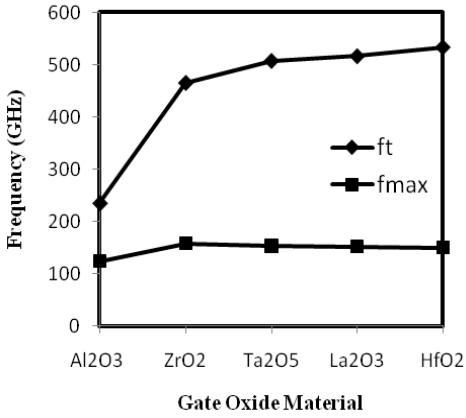

Fig.3.6 Impact of Gate Oxide Material on f_t and f_{max}

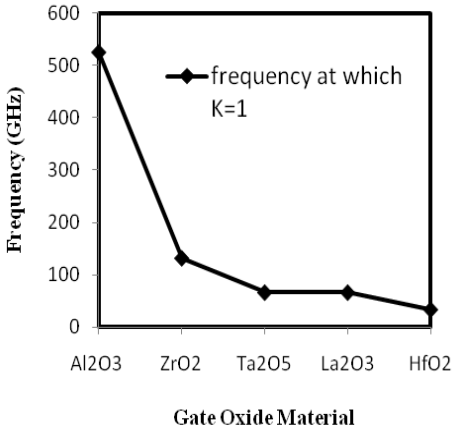

Fig.3.7 Impact of Gate Oxide Material on Frequency at which Stability Factor K=1

B. Impact of Gate Material

1) Gate Material Variation

The use of gate materials like Aluminium, Molybdenum and Tungsten show variation in tunnel FET behaviour. An increase in the on-current can be obtained with Aluminium as the gate material. Such a device also has higher f_t and f_{max}. Whereas, the device with Tungsten as the gate material is seen to have the lowest subthreshold swing.

Fig 3.8 shows the impact on I_{on} for various gate materials.

The variations in f_t and f_{max} can be seen in Fig 3.9. The impact on the frequency at which the stability factor K=1, can be visualised in Fig 3.10.

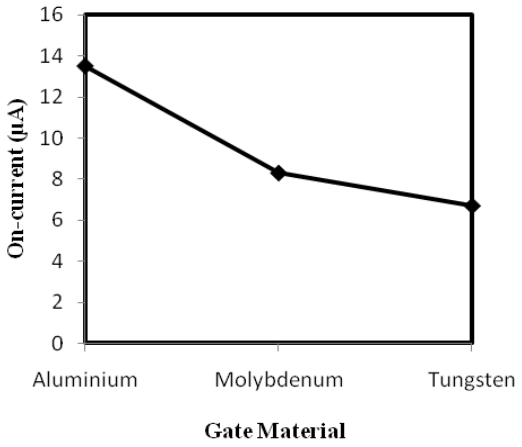

Fig.3.8 Impact on I_{on} for various Gate Material

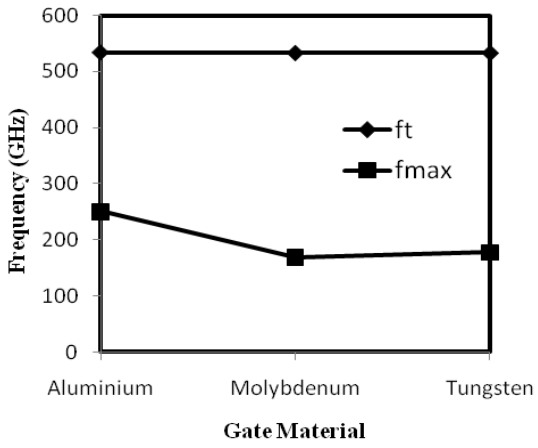

Fig.3.9 Impact of Gate Material on f_t and f_{max}

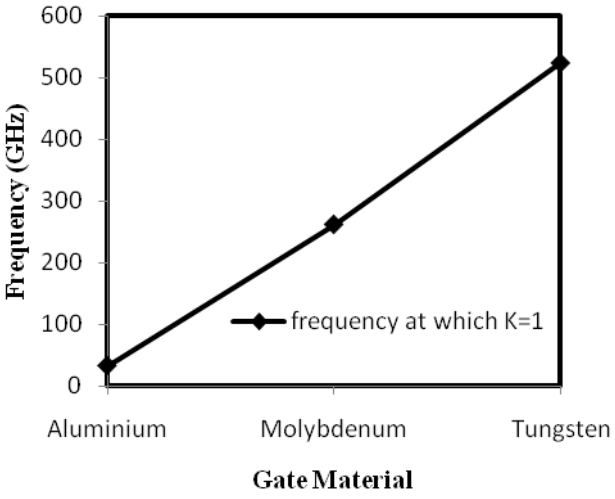

Fig.3.10 Impact of Gate Material on Frequency at which Stability Factor K=1

2) Gate Contact Alignment

Gate alignment is another important Tunnel FET design consideration. There have been recommendations to align the gate dielectric with the tunnel junction in order to take advantage of fringing and to shorten the gate on the drain end in order to increase device speed. The gate contact alignment variation also causes fluctuation in GAA-TFET dc characteristics, RF and stability performance.

The movement of gate towards the source shows good reduction in the off-current and subthreshold swing which is desired. It can be seen in Fig 3.11 and Fig 3.12 respectively. Both f_t and f_{max} have improved, which can be seen in Fig 3.13. Variations in the gate contact alignment have no impact on the stability of the device.

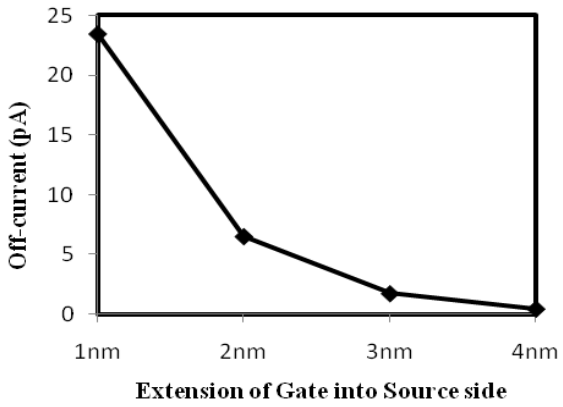

Fig.3.11 Impact of Gate Contact Alignment on Off-current

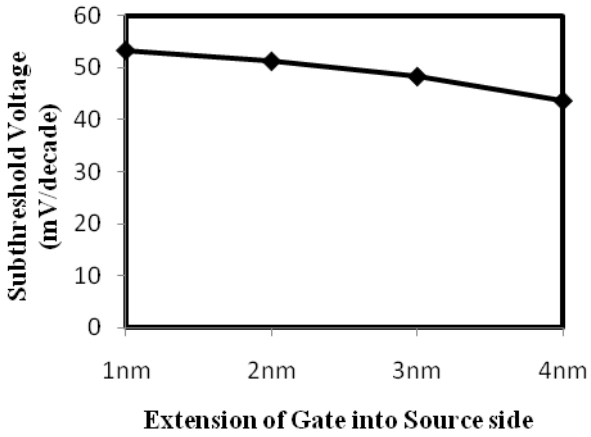

Fig.3.12 Impact of Gate Contact Alignment on Subthreshold Swing

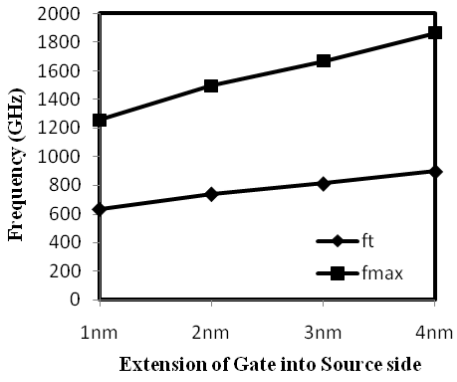

Fig.3.13 Impact of Gate Contact Alignment on f_t and f_{max}

IV. RF AND STABILITY PERFORMANCE OF OPTIMIZED GATE-ALL-AROUND TUNNEL FET

The RF performance of GAA TFET is evaluated by extracting f_t (cut-off frequency) and f_{max} (maximum oscillation frequency) which are known as the Figures of Merit (FoM) [7].

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It is necessary to observe the response of these FoM to understand the device behavior at high frequencies.

The f_t and f_{max} are the two parameters mainly responsible for estimating the high frequency performance of a RF device and can be defined theoretically as follows:

$$f_t = \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{max} = \frac{f_t}{\sqrt{4R_g(g_{ds} + 2\pi f_t C_{gd})}} \quad (2)$$

The cut-off frequency f_t is extracted when current gain is unity. From equation (1) it is observed that f_t increases as transconductance increases. The f_{max} is related to the capability of the device to provide power gain at large frequencies and is defined as the frequency at which the magnitude of the maximum available power gain, obtained under power-matching conditions at both the input and output ports drops to unity [8].

The values of f_t and f_{max} from the simulated results are 533GHz and 149GHz respectively which can be seen in Fig 4.1 and Fig 4.2 respectively.

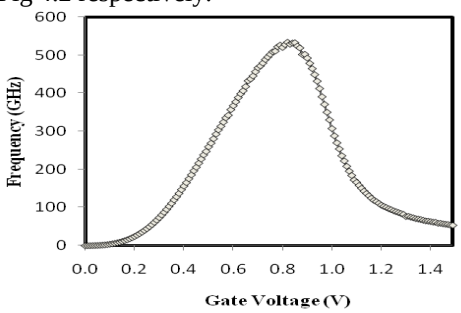

Fig.4.1 Cut-off Frequency as a function of gate voltage

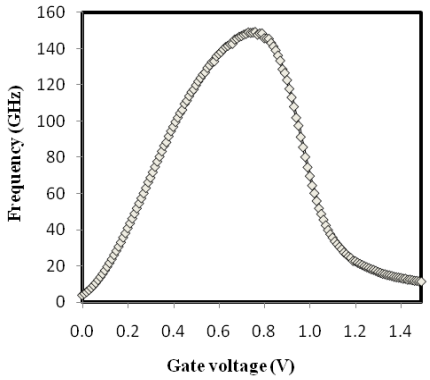

Fig.4.2 Maximum Oscillation Frequency as a function of gate voltage

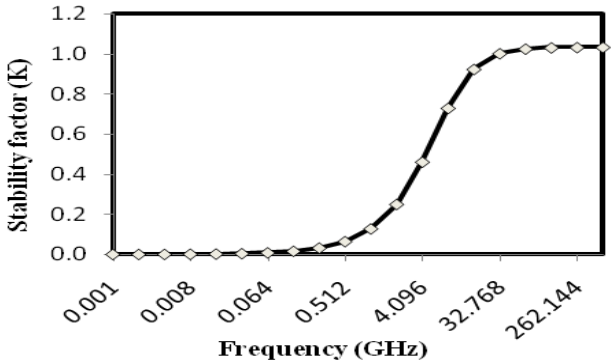

Fig.4.3 Stability Factor as a function of frequency

Stability of a device is determined by its stability factor (K). This factor gives an indication whether the device is conditionally/unconditionally stable. It must satisfy the condition K>=1 for a device to be unconditionally stable [9]. The stability factor in terms of Y-parameters [10] can be expressed as follows:

$$K = \frac{2Re(Y_{11})Re(Y_{22}) - Re(Y_{12} - Y_{21})}{|Y_{12} - Y_{21}|} \quad (3)$$

From Fig 4.3 it is found that the device is unconditionally stable from 32.8GHz onwards. When the device is unconditionally stable over a wide frequency range, it indicates that additional stability circuits are not required for RF circuits which reduce the circuit complexity.

V. CONCLUSION

The dc characteristics, RF and stability performance of GAA-TFET is presented using Silvaco TCAD simulation. The impact on the tunnel FET behaviour for various gate oxide thickness, gate contact alignment and doping concentration is also studied. It is seen that the optimal gate oxide thickness is 1nm and good results are seen when the gate is extended 4nm into the source side. The best doping levels for this device structure is: source- 1×10^{20}, drain- 1×10^{18} and intrinsic region- 1×10^{15}.

REFERENCES

1. Reddick W, Amaratunga GAJ. Silicon surface tunnel transistor. Appl Phys Lett 1995; 67:494.
2. Appenzeller J, Lin Y-M, Knoch J, Avouris Ph. Band-to-band tunneling in carbon nanotube field-effect transistors. Phys Rev Lett 2004; 93(19). 196805-1-4.
3. Boucart K, Ionescu AM. Double-gate tunnel FET with high-k gate dielectric. IEEE Trans Electron Dev 2007; 54(7):1725.
4. Bhuwalka K, Sedlmaier S, Ludsteck A, Tolksdorf C, Schulze J, Eisele I. Vertical tunnel field-effect transistor. IEEE Trans Electron Dev 2004; 51:279.
5. Zhang Q, Zhao W, Seabaugh A. Low-subthreshold-swing tunnel transistors. IEEE Electron Dev Lett 2006; 27(4):297.
6. Choi WY, Park B-G, Lee JD, Liu T-JK. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Dev Lett 2007; 28(8):743.
7. S. Cho, K. R. Kim, B.-G. Park and I. M. Kang. RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. IEEE Trans. Electron Devices, vol. 58, no. 5, pp. 1388–1396, May 2011.
8. R.Wang, J. Zhuge, R. Huang, Y. Tian, H. Xiao, L. Zhang, C. Li, X.Zhang, and Y.Wang. Analog/RF performance of Si nanowire MOSFETs and the impact of process variation. IEEE Trans. Electron Devices, vol. 54, no. 6, pp. 1288–1294, Jun. 2007.
9. G. Gonzalez. Microwave Transistor Amplifiers Analysis and Design. Englewood Cliffs, NJ: Prentice-Hall, 1997.
10. JM Rollet. Stability and power gain invariants of linear two ports. IRE Trans Circ Theory, Vol.9, 1962, pp. 29-32.
11. C. Sandow, J. Knoch, C. Urban, Q.-T. Zhao, S. Mantl. Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors. Solid-State Electronics, 53, 1126–1129, 2009.