RF Bluetooth LNA Test Cost Reduction for Catastrophic and Parametric Faults

Ayari Nadia, Hamdi Belgacem

Abstract: ***Radio Frequency and Analog circuit are often tested based on their performances. In this paper we investigate the test of RF Bluetooth LNA design for catastrophic and parametric fault model. The proposed technique is based on the measurement of S-parameters, Noise Figure, factor of stability, third-order intercept (IIP3) and the current consumption. The purpose of this study is reducing the test sets while keeping high fault coverage. The efficiency of this technique is proved by fault injection on the LNA circuit, measurement of parameters and analysis of fault coverage in each case. This study shows that we obtain acceptable fault coverage with reduced set of parameters. Two parameters are sufficient for parametric faults to get 98.7% fault coverage. For catastrophic fault we obtain 100% fault coverage with only three parameters.***

Keywords: ***LNA, Noise Figure, IIP3, factor of stability, S parameters, test, fault coverage.***

I. INTRODUCTION

The test cost of RF-integrated circuits and systems can be as high as 40% of their manufacturing cost [1] and there should be a low cost way to test cost *RFIC* chips for SOC. However the reduction of test cost of RFSOC still remains to be the major bottleneck to make affordable wireless systems. The problems come from the difficulties in RF SOC testing due to the limited access to major components of internal RF structures and the non-linear effects in RF faults may cause on a circuit under test [2-5]. There are many techniques of test based on Built in Self Test (BIST) proposed for testing RF and analog circuits. First in this paper, we describe 2.4-2.5 GHz-band CMOS LNAs optimized for Bluetooth application. Our purpose is to improve the performance of LNA. The emphasis of this study is to reduce the power consumption of the CMOS LNA while still retaining acceptable noise performance, good input/ output match, sufficient linearity, and a high dynamic range. A cascode amplifier topology with inductive degeneration at the source was used. The LNA offered NFs of 1.98dB and input return

Losses of-11dB, output return losses of -44.69dB, input ICP1 of -10 dBm and IIP3 of 5 dBm with power consumptions of 7.33 mW. Then, we detail the models of faults. After we show the result of injection of fault and their effects on the S parameters, noise figure, factor of stability, IIP3 and current consumption Icc. Finally a conclusion about the work is done.

II. DESIGN CIRCUIT

In [6], results of a supply current testing methodology are presented. This technique is based on measuring current consumption of integrated circuits as a matter of testing and observing the corresponding current signatures. In [7], a testing technique is presented for selecting multiple power supply levels and observing the corresponding quiescent current signatures. In this work an essential measurement of parameters is used in order to detect catastrophic and parametric faults. We consider, also faults for passive components and MOS transistors.

Figure 1 shows a schematic of a source–inductor–feedback amplifier with the gate inductor for input impedance matching. The source inductor is used to achieve simultaneous input and noise matching [8]–[9] and to provide the desired input resistance 50Ω [10]. The Cascode is a combination of a common-source device (ie our LNA) with a common-gate load. This has the effect of increasing the output impedance. The additional cascode device has been configured as a diode. The inductor between the cascode source and supply blocks any RF is leaking to the supply rail and may be varied in value to optimize the gain response of the LNA.

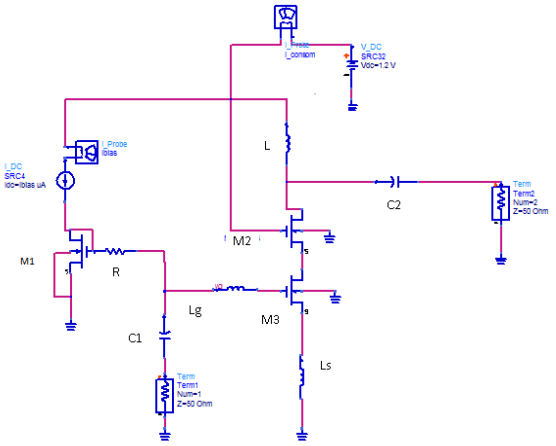

Fig. 1: Schematic of a Source Inductive Degeneration LNA

The LNA offered NFs of 1.98dB, input return losses of-11dB, output return losses of -44.69dB, input ICP1 of -20 dBm and IIP3of -3 dBm with power consumption of 7.33 mW.

Simulations were done using 0.13 um CMOS process. The amplifier provides a maximum gain of 20.343 dB as shown in figure 2. Cgs and gm are selected according to (1) to make the input matching Zin as possible to 50 Ω.

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Ayari Nadia, Department of Electronic & Microelectronics' LAB. Monastir, Tunisia, Email id: ayarinadia13@yahoo.fr.

Belgacem Hamdi, Department of Electronic & Microelectronics' LAB. Monastir Tunisia, Email id: belgacem.hamdi@gmail.com.

Zin=s(Lg+Ls)+1/sCgs+gm/CgsLs≈s(Ls+Lg)+1/sCgs+WL(1)

to achieve input matching, the Zin should be 50 Ω, so

$$Zin=gm/Cgs\ Ls \quad (2)$$

The value of Ls is picked and the values of gm and Cgs are calculated to give the required Zin.

This circuit operated with 1.2 V supply. The reverse isolation S_{12} (Fig.3) is good with more than -44 dB. A minimum noise figure of 1.98 dB and 3.0 dB are obtained around the desired frequency 2.4-2.5 CHz for the designed LNA's as shown in figure 4. This is due to the use of the cascode configuration. The Simulated results of ICP1 and IIP3 are shown in Figure5 with respectively -10 dBm and 5 dBm.

These results demonstrate that high dynamic range and good linearity has been also achieved. The performance of our CMOS LNA are the best reported values among the 2.4-2.5 GHz band CMOS LNA's compared to some other characteristics in Table I. According to the meaning of the stability figure K >1 the circuit is stable unconditionally.

TABLE I. Classical Values for MOS LNA

Author [Ref]	NF (dB)	Gain (dB)	IIP3 (dBm)	Power (mW)	F0 (GHz)
Shaeffer [10]	3.5	22	-9.5	30	1.5
Rafla [11]	2.5	22	-10	12	2.5
Huang [12]	3	19.8	4.5	22.4	2.4
Yang [13]	2.2	15	1.3	7.2	2.4
Tinella [14]	3	13.4	0	4.5	2.5
Li [15]	2.88	15.9	0.2321429		2.45
Lagnado [16]	2.2	11	3	13.2	2.4
This work	1.98	20.343	5	7.33	2.4-2.5

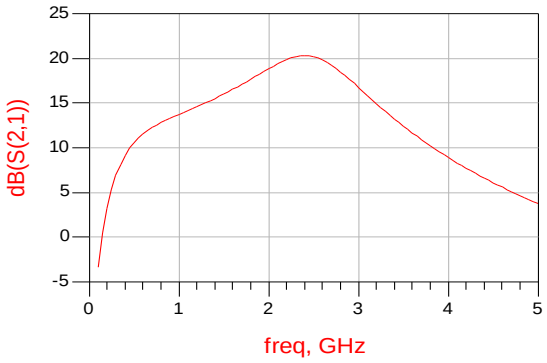

Fig. 2: Simulated Characteristics of Gain (S_{21})

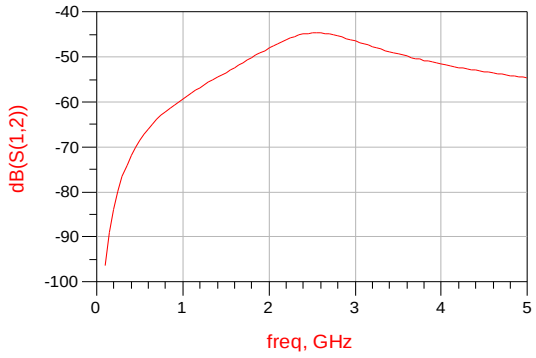

Fig. 3: Simulated Characteristics of Reverse Isolation (S12)

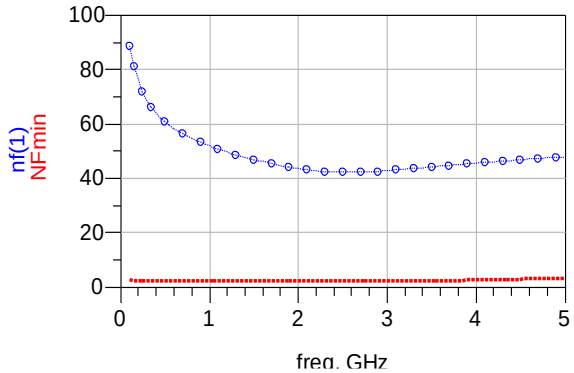

Fig. 4: Simulated Noise Figure and Minimum NF

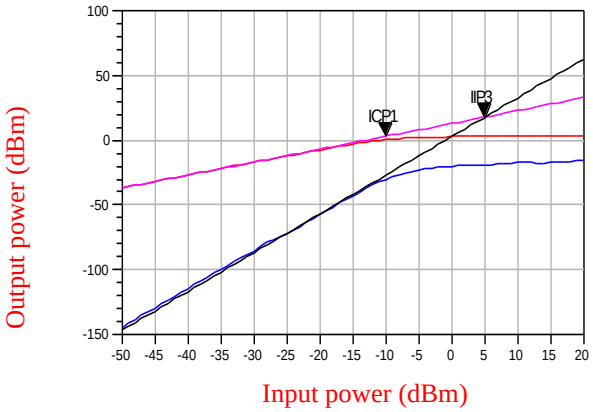

Fig. 5: Simulated Compression Point (ICP1) and IIP3

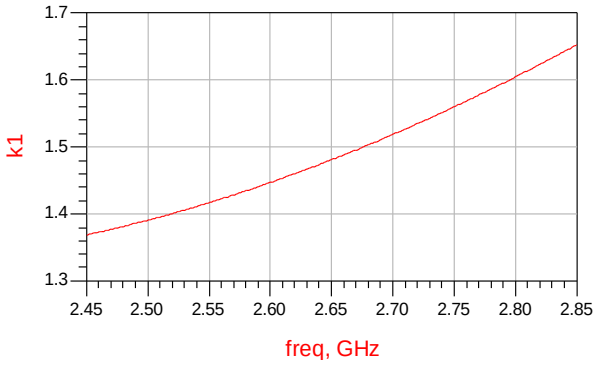

Fig. 6: Simulated Stability Figure K1

III. MODELS OF FAULT

Faults can be classified into two categories in analog and RF circuit: catastrophic (hard) and parametric (soft).

- Catastrophic Fault Models

Catastrophic faults include generally shorts between nodes, open nodes and other changes in a circuit. The catastrophic fault models consist of open faults (OF) or resistive breaks, short faults (SF) or resistive bridges [17]-[18]. We considered three different catastrophic faults for the MOSFET such as drain to source (D-S), gate to source (G-S) short fault and gate open fault as shown in figure 7.

For each transistor, short-circuits between the terminals (Grille-source) with a resistor value of 1 Ohm and opens with a value of resistor in grille of 10MΩ (fig 7) have been considered.

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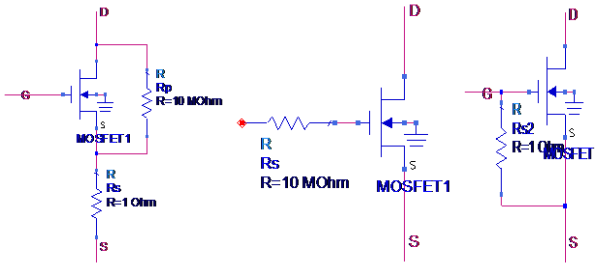
For capacitors, inductors and resistors, component shorts and opens have been included. For Opens Fault Resistors have been modeled with a resistance value of 10 *R and shorts with a resistor of 0, 1*R as shown in figure8. In Figure 9 Capacitors are open by a value of 10*(WC) and has been shorted by 0, 1/ (WC). Inductors was modeled with 10* (WL) for open fault and 0, 1 / (WL) for short fault (fig.10).

We can establish from the fault model an equation to calculate the number of catastrophic faults simulated for integrated circuit CMOS:

$$NFC = 3*(R+L+C+M) \quad (3)$$

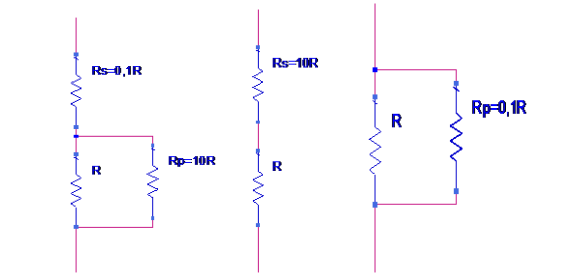
With NFC is the number of catastrophic faults, R the number of resistors, C the number of capacitors, L the number of inductors and M the number of transistors. Each fault has been simulated independently from each other.

The catastrophic faults resulting from circuit shorts, open and free fault. Circuit components include MOSFETs transistors, capacitors, inductors and resistors.



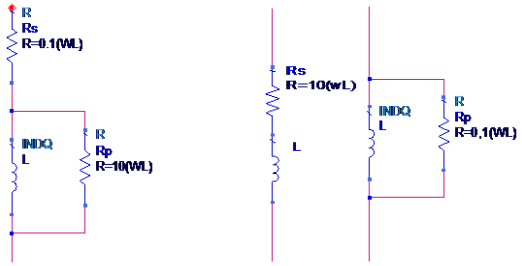
(a) Fault- Free (b) Open (c)G-S short

Fig. 7: Fault Models of MOSFETS



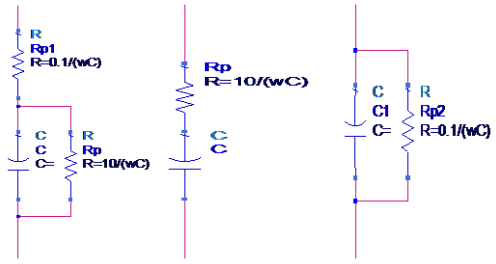
(a) Fault-free (b) Open (c)Short

Fig. 8: Fault Models of Resistors



(a) Fault-Free (b) open (c) Short

Fig. 9: Fault Models of Inductors



(a) Fault-Free (b) Open (c) Short

Fig. 10: Fault Model of Capacitors

- *Parametric Fault Models*

Parametric faults are a result of a random fluctuation or a variation in parameters such as process variation and thermal variation [19-20]. This fault leads to a significant performance loss that violates the circuit specification. It is concerned with a parametric fault since this fault is hard to distinguish from acceptable process variations [20]. We considered faults parametric for passive components and MOSFETs transistors.

We considered ±10% to ±50% variations in resistors, capacitors and inductors. For MOSFETs ±25% and ±50% channel length and width variations are considered. 77 faults models have been considered for the LNA's components.

IV. FAULTS SIMULATION RESULTS

This part resumes the result obtained by simulation according to injection of catastrophic fault. The detected faults are classified into three types (shorts, opens and free fault). The sensor detects 100% of the simulated shorts and opens fault in LNA.

Thus, current consumption allows the detection of 100 % of the faults for opens and shorts transistor. S parameters are detected by capacitor open, short and free fault but Capacitor has no impact on the NF parameter. All S parameters have fault coverage of 100 % of resistor short faults. We can test one of S parameters mainly the time of the simulation is the same. For inductor only free Fault not detected.

Figure 11 shows the catastrophic fault coverage for all test parameters is detected. All S parameters and Noise Figure have detected and have 96% fault coverage. Current consumption (Icc) gives a fault coverage of 74%. IIP3 and Factor of stability has more than 70% test coverage.

With these results we can only three parameter specification of the circuit. The combined fault coverage of the three parameters is about 90%. When S21, Icc and IIP3 are tested we obtain a 100% fault coverage. Fault coverage comparisons are shown in Figure 11 where:

Total1 = FC (Icc, S_{21}, NF)	96.2%
Total2 = FC (Icc, S_{11}, k1)	92.6%
Total3 = FC (Icc, S_{21}, IIP3)	100%
Total4 = FC (Icc, S_{22}, NF)	85.15%

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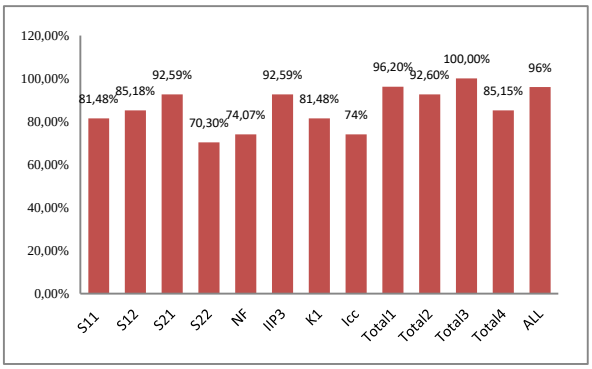

Fig. 11: Catastrophic Fault Coverage

As shown in Figure 12, S_{11} and I_{cc} have the highest parametric fault coverage (87.7%). S12 has the lowest fault coverage. The Noise Figure has not always detected and has fault coverage of 59.48%. The current consumption gives fault coverage of 87%. With these results of parametric fault we can test only one of S parameters and the current consumption Icc. The combined fault coverage of the two parameters is more than 96%. When S21 and Icc are tested we obtain a 98.7% fault coverage. Fault coverage comparisons are shown in Figure 12 where:

Total A= FC (Icc, S_{12}) 96.1%
Total B= FC (Icc, S_{11}) 97.4%
Total C= FC (Icc, S_{21}) 98.7%
Total D= FC (Icc, S_{22}) 96.1%

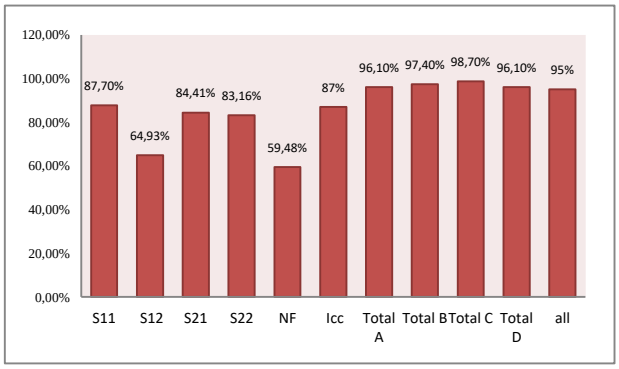

Fig. 12: Parametric Fault coverage

V. CONCLUSION

The measurement of all performance parameters that are specified for analog and RF circuits requires long test time and numerous test setups.

In This paper, we investigate the impact of association of a reduced set of test parameters, on the fault coverage. The fault coverage was estimated according to a large set of faults including parametric and catastrophic fault model. This study demonstrates that we can reduce the test cost by reducing the number of test parameter with good fault coverage. For catastrophic fault showed that we reach full coverage (100%) with only Icc, S21 and IIP3 parameters testing. We had also, shown that for parametric fault model that the fault coverage was more than 96% considering only two LNA parameters. For example the couple (Icc, S21) guaranteed 98.7% fault coverage.

As a future work, we can plan the employment of the proposed test approaches and analyses for others RF designs to reduce test cost of such systems.

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