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Design & Analysis of Low Power Low Voltage Regulated Cascode Current Mirror

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Abstract*: The current mirror is core structure of all most all analog and mixed mode circuits and the performance of analog structures largely depends on their characteristics. In this paper first we study the simple current mirror, cascode current mirror and different low voltage current mirror topology and study the literature survey advantage and disadvantage. Second we study , analysis and design of convention regulated cascode current mirror, regulated cascade current mirror,wide output swing regulated cascade current mirror and wide input output swing regulated cascode current mirror and simulate Tanner EDA tool T-SPICE 0.18µm CMOS technology. Presented analysis low voltage current mirror input characteristic, output characteristics high output swing capability and wide input and wide output swing capabilities, suitable for low voltage operation and minimum power dissipation .

Index Terms*: low voltage current mirror , level shifted current mirror , cascode current mirror , WIOS -RCCM

I. INTRODUCTION

Accurate analog signal processing requires ideal circuit operation. The current mirror is one of the Most building blocks it both in analog and mixed mode VLSI circuit[6]. In current mod circuit, the current mirror –current controlled current source determines the overall performance of the system. Now day's rapid development of communication and computer, chips are required more and more to small size. Today large electronic component constructed mostly with digital design techniques, many systems still have analog components[1] .Current mirror is a core structure for all most all analog and mixed circuit determines the performance of analog structuress which largely depends on their characteristics ,input output resistance ,input linear range, output voltage swing, DC-balance, dynamic range, finite bandwidth, device matching .for low voltage currents mirrors are mandatory with high performance ,the accuracy and output impedance are the most important parameters to determine the performance of current mirror ,current mirror is another importance parameter in dynamic range enhancement application is dynamic range .it has to be able to operate at high frequency with low power supply voltage and low input /low output voltage requirement. The dynamic range is determined by the ratio of maximum signal level (at specified level of distortion) to the minimal detectable signal level[4]. The minimum detectable signal is referred in current mode circuits; the input noise current and maximum signal current is determined by the input linear range. Most current mirrors are usually desired to have high output impedance, and large output voltage signal swings, there is some application where having large input voltage signal swing and large output voltage swing. Application of current mirror implementation of VLSI test circuits, Reducing the level of phase noise in the output spectrum ,Low power integrator bio amplifier, Radio-frequency (RF) circuits, Baseband signal processing, Sensors on a same chip.

II. TOPOLOGY OF CURRENT MIRROR

A. Simple current mirror

Figure1.1a. shows a conceptual means of copying current. The design of current source in analog circuits is based on copying current from a reference, with assumption that one precisely-defined current source is already available. For a MOSFET, if drain current $I_D = f^{-1}(V_{GS})$, where f(.) denotes the functionality of I_D verses V_{GS} ,then $V_{GS} = f^{-1}(I_D)$,that is if the transistor is biased at I_{REF} then it produces $V_{GS} = f^{-1}(I_{REF})$ as shown in figure 1.1b.Thus if this voltage is applied to the gate and source terminals of a second MOSFET, the resulting current is $I_{out} = ff^{-1}(I_{REF})$

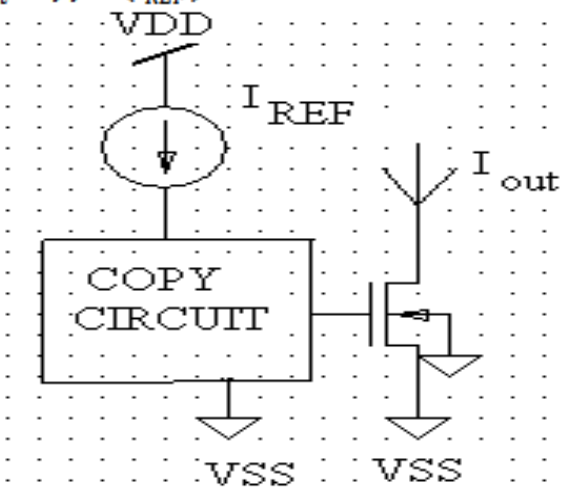

Figure 1.1a: Conceptual means copying currents

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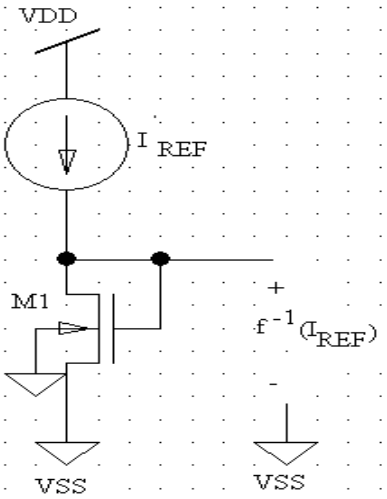

Figure 1.1b: Diode connected device providing inverse function

From another point of view ,two identical MOS devices that have equal gate –source voltages and operate in saturation carry equal current(if λ=0). The structure consisting of M1 and M2 in figure 1.2 is called a "Current Mirror" in the general case; the dimensions of transistors in current mirrors need not be identical [2].

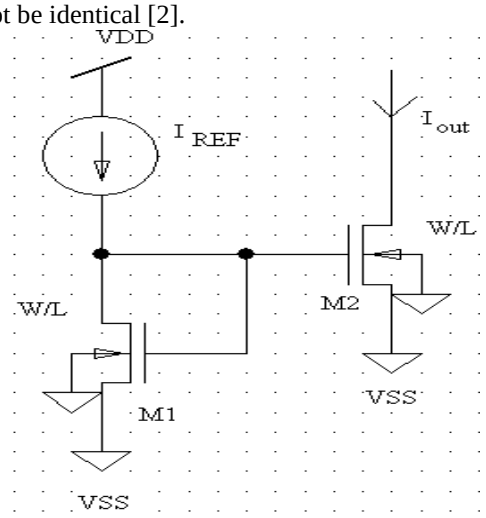

Figure 2: Basic Current Mirror [2]

Neglecting channel length modulation, we can write:

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{tn})^2, \quad (1)$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{tn})^2 \quad (2)$$

Resulting in,

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}. \quad (3)$$

The key properties of this topology are that it allows precise copying of the current with no dependence on process and temperature. The ratio of I_{out} and I_{REF} is given by the ratio of device dimensions, a quantity which the designer can be control with reasonable accuracy [4].

B. Cascode Current Mirror

Basic four transistors NMOS types M_1, M2, M_3 and M_4 are constructed in cascode current mirror, channel length modulation are neglected, this effect results insignificant error in copying currents in this circuit, negative feedback is also involved. In figure 2.5 M4, shields M_2 from the variation in voltage that occurs at the output terminal, namely V_o a simple explanation is that both V_g and V_g remain constant, while Id_4 tends to increase on account of an increase of V_{out} and this requires that Id_2 increases too. Consequently, V_{ds2} will rise and V_{gs4} will fall so that I_o stays nearly constant. Cascode current mirror enable more precise current mirroring because the drain voltage of transistor M1, M2 is imposed by the cascode transistors. It is used as an active load for cascode or folded differential pairs, since it provides high output resistance. The cascode transistors demand an additional voltage bias it is usually calculated in the same way as for the cascode structure transistor by keeping the bottom transistor at the limit of saturation.

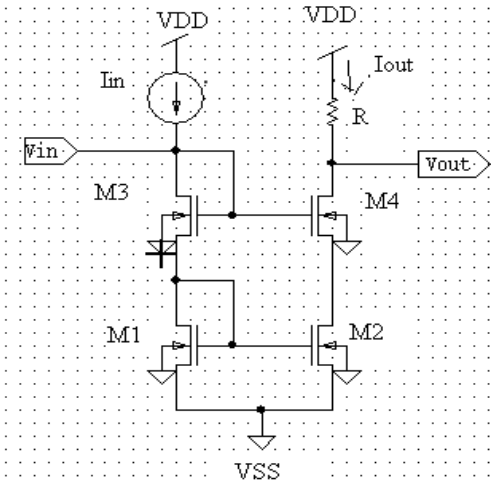

Figure 3: Cascode Current Mirror [4]

Advantage

- An important advantage of cascode transistor does not contribute to the equivalent input noise and offset of amplifier.
- Minimum input voltage, Challenge for low voltage design.
- Achieves very high output gain.
- Minimum output voltage.

C. Triode region cascade current mirror

Triode region based MOSFET current mirror shown in figure 4 transistors M1 and M2 operated in triode region. When we assume transistor M1 and M2 are active resistors then the circuit analyzed as Widlar current source. The active degeneration resistors increase the output impedance. The CM provides cascode type out put impedance. Transistor M4 and M5 are diode connected and transistor M4 is used to bias the transistor M5 [3].

1. Transistor M3 and M4 will operate in triode region if the input current is sufficiently less than biasing current for M5.
2. The structure may not be suitable for high frequency applications.

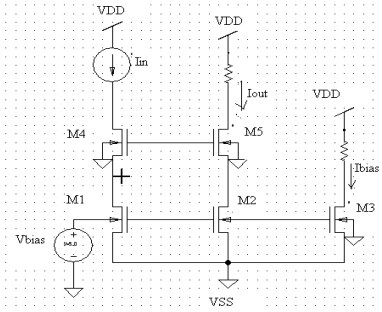

Figure 4: Modular Current Mirror [3]

D. Wide swing current Mirror

Cascade current mirror of figure 5 drain of M2 is held at the same potential as the drain of M1 that is V_{GS} or $\sqrt{(2IREF)}/_{\beta}$ before it starts to enter the triode region.

Wide swing means the maximum voltage across the current mirror is $2\sqrt{\frac{(2IREF)}{\beta}}$ the sum of access gate voltage of M2 and M4. The operation of this circuit, assume that M1 through M4 have the same $W/_L$ ratio their βs are all equal we know that the V_{GS} of M1and M2 is $2\sqrt{\frac{(2IREF)}{\beta}}+V_{THN}$. It is desirable to keep M2 drain at $2\sqrt{\frac{(2IREF)}{\beta}}$ for wide swing operation , this means, since M3/M4 are the same size as M1/M2 , the gate voltage of M3/M4 must $V_{GS}+\sqrt{\frac{(2IREF)}{\beta}}$ or $2\sqrt{\frac{(2IREF)}{\beta}}+V_{THN}$ .By using M5 channel width so that it is one fourth of the size of the other transistor width and forcing I_{REF} through the diode connected M5 we can generate this voltage .we should point out that the size (its $W/_L$ ratio) of M5 can be further decrease, say to $1/_5$, in order to keep M1/M2 from entering the triode region (output resistance decreases) .The cost is an increase in the minimum allowable voltage across M1/M4,that is, V_{OUT} .

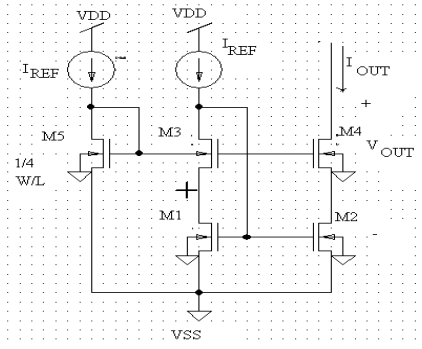

Figure 5: Wide Swing Current Mirror

Advantages:

- Higher output voltage swing than cascode current mirror.
- Higher output impedance.

Disadvantage:

- Use additional bias circuit (power consumption).

E. Self cascode low voltage current mirror

Self cascode low voltage current mirror shown in figure 6, M1 & M2, M3 & M4, M7 & M8 are pairs of composite cascode structures. Ibias3 and Ibias4 are assumed to be 1nA and 100µA respectively. The selection criterion for Ibias3 is to ensure lower Vin. Ibias4 is selected to ensure ON condition for M6. All the circuit operations are simulated for supply voltage of $\pm$0.5 V [13].

Advantage:

Self cascode LVCM a high performance current sink and source having an output resistance of 9 MΩ. This approach of increasing the (*W/l*) aspect ratios works effectively at low bias voltage V_{in} of $\pm$0.5 V. Its high bandwidth (6.02 GHz) without any additional components makes it quite attractive for biasing analog circuits requiring high output resistance and gain. Hence this can be used as load resistances in CM circuits. They can extensively be used where power supply requirements are not the constraint and that high output resistance is of outmost importance [13].

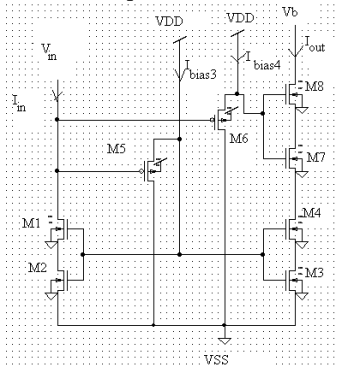

Figure 6: Self Cascode Low Voltage Current Mirror [13]

III. LOW VOLTAGE CURRENT MIRROR

One of the most fundamental building blocks of analog integrated circuit is the Low Voltage current mirror .Current mirror is enable a single current source to supply mirrors are output impedance and voltage headroom. The output impedance determines the variation of the mirrored current when the applied voltage varies. Higher output impedance implies less current variation with applied voltage and hence a more stable current source Voltage headroom specifies how much voltage drop across the current mirror is required ton operate the current mirror reliably. This is especially important for low voltage circuit design.

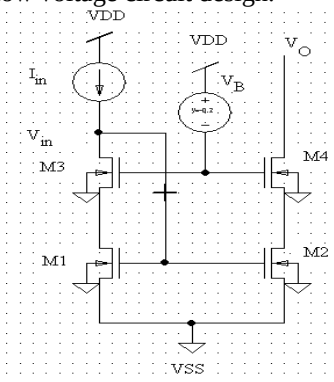

Figure 7: Low Voltage Current Mirror

The low voltage cascode current mirror shown in figure 3.4 .We assumes that the current mirror transistors M1 and M2 have identical, aspect ratio.$A_M = \frac{W_1}{L_1} = \frac{W_2}{L_2}$ Where W_1

and W_2 are the transistor channel width and L_1 and L_2 are the transistor length. Similarly the transistor M3 and M4 are assumed the same aspect ratio $A_C = \frac{W_3}{L_3} = \frac{W_4}{L_4}$ .The aspect ratio A_M may be different from the aspect ratio A_C . In the analysis of the dynamic range the same aspect ratio of A_M and A_C and we use standard Schman –Hodges transistor model for the transistor in the saturation region and we neglected the bulk effect and assume that all the NMOS transistors have the identical. Low voltage current mirror input current I_{in} we find the gate- source voltages and drain -source voltages

$$V_{GS1} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_M}} \quad (4)$$

Gate to source voltage of transistor M3

$$V_{GS3} = V_{tn} + \sqrt{\frac{2I_{in}}{KA_C}} \quad (5)$$

Drain to source voltage of transistor M1 is

$$V_{DS1} = V_{BC} - V_{tn} - \sqrt{\frac{2I_{in}}{KA_C}} \quad (6)$$

Drain to source voltage of transistor M3 is

$$V_{DS3} = V_{GS1} - V_{DS1}$$

$$= 2V_{tn} - V_{BC} + \sqrt{\frac{2I_{in}}{K}}\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}} \quad (7)$$

Where, V_{tn} is the transistor threshold voltage, V_{BC} is the bias or gate voltage of transistor M3 and M4 and K is the transconductance parameter. Requiring $V_{GS} - V_{tn} \leq V_{DS}$ for both M1 and M3 result in:

$$\sqrt{\frac{2I_{in}}{K}}\left(\frac{1}{\sqrt{A_M}} + \frac{1}{\sqrt{A_C}}\right) + V_{tn} \leq V_B \quad (8)$$

Biasing voltage:

$$V_B \leq 2V_{tn} + \sqrt{\frac{2I_{in}}{K\,A_M}} \quad (9)$$

In figure 7 low voltage current mirror, biasing voltage V_B is fixed when I_{in} increases, voltage of the gate –source voltage V_{GS3} of transistor M3 and V_{in} will increase, and voltage level at the drain terminal of M1 decreases. There by M1 enter the triode region which determine upper limit of I_{in} .Below equation (3.9) ensure the saturation of M1 and determines the maximum value of I_{in} for given value of the cascode bias voltage V_B we find

$$I_{in,max} = \frac{K}{2} A_M (V_B - V_{tn})^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2$$

(10)

Equations (10) ensure the saturation of M3 and determine the minimum value of I_{in}. We find

$$I_{in,min} = \frac{K}{2}(V_B - 2V_{tn})^2 A_M \quad (11)$$

Maximum value of the bias voltage even at the minimum value of input current equation (11) determine, and equation (11) determined the value of A_C and A_M which determined the saturation of M1 and the maximum value of input current . To ensure Saturation operation of transistors M1 and M3 the input current range determined by

$$\frac{K}{2} A_M(V_B - 2V_{tn})^2 \leq I_{in} \leq \frac{K}{2} A_M(V_B - V_{tn})^2 \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2$$

(12)

In a practical design procedure equation(11) can be used to determine the maximum value of the bias voltage which will ensure saturation of M3 even at the minimum value of input current, and equation (10) can then be used to determine values of A_C and A_M which will ensure saturation of M1, even at the maximum value of input current.

In the important special case of $I_{in,minimu} = 0$ we find from (3.10) $V_B \leq 2V_{tn}$. From equation (10) we then find the following design constraint on A_C and A_M

$$A_M \left(\frac{\sqrt{A_C/A_M}}{1+\sqrt{A_C/A_M}}\right)^2 \geq \frac{2I_{in,max}}{V_T^2 K}$$

(13)

Assuming as a typical case W1 = W3 and L1 = L3 i.e. identical aspect ratios for the mirror transistors and the cascode transistors, we find

$$A_M = A_C = \frac{W}{L} \geq \frac{2I_{in,max}}{V_T^2 K} \quad (14)$$

In this case the effective gate-source voltage of the mirror transistors M1 and M2 is

$$V_{GS1} - V_{tn} = \sqrt{\frac{2I_{in}}{KA_M}} = \frac{V_{tn}}{2}\sqrt{\frac{I_{in}}{I_{in,max}}} \quad (15)$$

In this case the minimum output voltage of the current mirror is and is independent of the input current.

$$V_{out,min} = V_B - V_{tn} = V_{tn} \quad (16)$$

In a high precision current mirror one would like to have as large an effective gate-source voltage as possible in order to minimize the effect of threshold voltage mismatch.

IV. LEVEL SHIFTED CURRENT MIRROR

level shifted current mirror shown in figure 8. Level shifted current mirror operates at low voltage with the advantage of low input output voltage requirement, incorporates a level shifter PMOS transistor M5 (biased through a current I_{bias1}) at input port. For this structure, we have

$$V_{DS1} = V_{GS1} - V_{GS5} \quad (17)$$

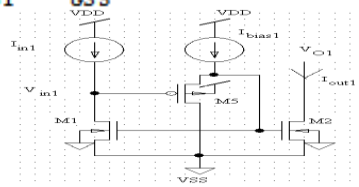

Figure 8: Level Shifted Current Mirror

Where V_{DS1} drain to source and V_{GS1} gate to source voltage of M1, V_{GS5} is the gate to source voltage of M5. A level shifted current mirror circuit structure is shown in figure 8 M3 is used to shift the voltage level at the drain terminal of M1. V_{in} is a characteristics parameter of a low voltage current mirror and decides the range of input voltage swing in such circuits. The bias current (I_{bias1}) decide the operation region of M1. For example, low value of I_{bias1} forces M3 to operate in sub threshold region, I_{bias1} high I_{bias1} ensures M5 operates the triode region. For high value V_{DS2}, M2 operates in saturation region. Gate voltage of M1 is high correspondingly input current is also high. Thus V_{in} can be calculated for this circuit structure if we know the values of V_{GS1} and V_{GS5} since $V_{tp} > V_{tp}$, there is a difficulty to keep the condition $V_{GS1} - V_{GS5} > 0$ valid in a level shifter based circuit over a wide range of I_{in}. One of the solutions is to use a lateral p-n-p transistor for level shifting, and now $V_{in} - V_{GS1} - V_B > 0$ approximates as 0.7V and V_{GS1} is always more than 0.8v (if we assume V_{tn}=0.8v). As the device sizes are reducing and V_t is also reducing and there will be a situation where $V_{GS1} - V_B > 0$ will not be valid and hence we may not be able to use p-n-p transistor. Thus, there is a need to have an alternative a p-n-p transistor and the use of a PMOS transistor is the most obvious choice. Thus it becomes necessary to discuss various possible modes of operation in this circuit and to identify the suitable modes, which result in the desirable properties for the resultant low voltage current mirror structure. Before I discuss them I invoke various equations, which describe the drain current of a MOSFET in various regions.

All symbols have usual meanings. There may be much possible combination in which transistor M1, M2 and M5 can be operated such as

1. M1 and M5 operated in sub- threshold.
2. M1 operating in saturation region and M5 operating in sub- threshold region.
3. M1 and M5 operating in saturation region.

The most suitable operational mode now is operation of M3 in sub-threshold region while M1 operates in sub-threshold region for low input currents and in saturation region for high input currents. The following analysis assumes that M3 operates in sub-threshold region while M1can operate in sub-threshold and/or saturation region. The necessary conditions for these operations are the current through M3 should be small enough to keep M3 in sub-threshold region. Correspondingly W/L ratio should be large. The current through M1 should be large to keep it in saturation region. However when input current will be low it will operate in sub-threshold region.

V. REGULATED CASCODE CURRENT MIRROR

A. Conventional Regulated Cascode current mirror

Regulated cascode technique greatly increases the d.c. gain of cascode amplifier without sacrificing speed or output swing [11]. As shown in figure. 9 the drive transistor M1 converts the input voltage V_{in} into a drain current that flows through the drain-source path of M2 to the output terminal. To mitigate the effect of channel length modulation (λ) of M1, its drain-source voltage must be maintained at fixed voltage level. This can be accomplished by a feedback loop consisting of an amplifier and M2 as source follower, thereby increasing the output resistance (ideally infinite), hence the d.c. gain. M2 shields M1 from possible variations of drain-source voltage [18]. In the simpler form the feedback amplifier is implemented by a common-source amplifier consisting of M3 and I_a figure 3.7. A problem with regulated cascode structure of figure 9 is that the minimum level of output swing is limited, because drain-source voltage of M1 never touches $(V_{GS} - V_{tn})$ a minimum required voltage to keep M1 in saturation. As

$$V_{out(min)} = V_{ds1} + V_{ds2(min)} = V_{gs3} + V_{ds2} \quad (18)$$

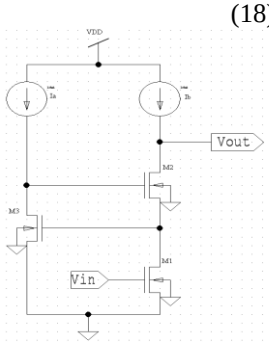

Figure 9. conventional regulated cascode current mirror

because $V_{ds1} = V_{gs3}$, which should be at least $V_{tn3} \approx$ 0.4v for 250nm TSMC CMOS process. However M1 can still remain in saturation with few hundredths of volt as its drain-source voltage. Thus, voltage requirement above $V_{ds1(sat)}$ is shear wastage, which limits the output swing and the minimum supply voltage.

Application: A regulated cascode current mirror is commonly used to maximize the output impedance. RCM offer the desired high output impedance. Uses of an operational amplifier enhance the regulated cascade current source. Uses of operational amplifier enhance the compliance voltage which can make the design more suitable for low voltage application.

B. Regulated cascode current mirror

A regulated cascode structure behaves like a MOS transistor with higher *Rout* and improved frequency response [4]. Figure 10 shows current mirror constructed by utilizing 'transistor like' (shaded area) regulated cascode structure. Although, this structure gives improved characteristics due to V_{ds} matching of drive transistors, it does not change the input and output compliance voltage, thus prevent low voltage operation. A solution to this problem is provided in [6] that enhance the input signal swing capability in addition to adaptive biasing to facilitate low voltage operation. We tried this technique along with the proposed [9] wide output swing regulated cascode structure figure 9, as a result a wide input and output swing current mirror with improved characteristics is obtained.

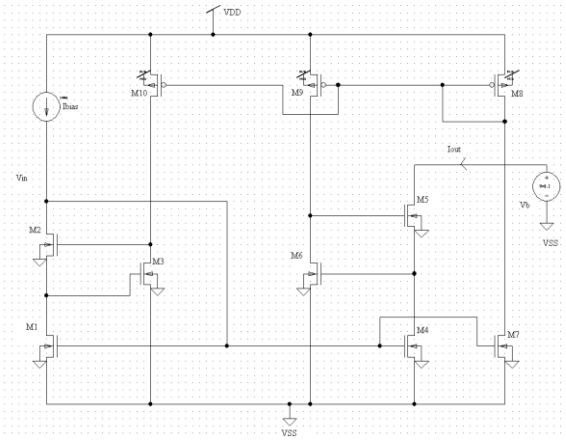

Figure 10: Regulated Cascode Current Mirror

VI. WIDE OUTPUT SWING REGULATED CASCODE CURRENT MIRROR

Wide output swing regulated cascode current mirror in prposed[7] Simulation of the modified CM structure of Figure 11 provides excellent output characteristics and almost ideal matching of currents with high input current range from approximately 1nA to 750µA. However, input compliance voltage remains same which limits input voltage swing at 1V supply. Therefore, we tried by replacing "transistor like" structure at the input with that of a single transistor and a level shifter as proposed in [11]. The resultant structure thus provides wide swings at input as well as output.

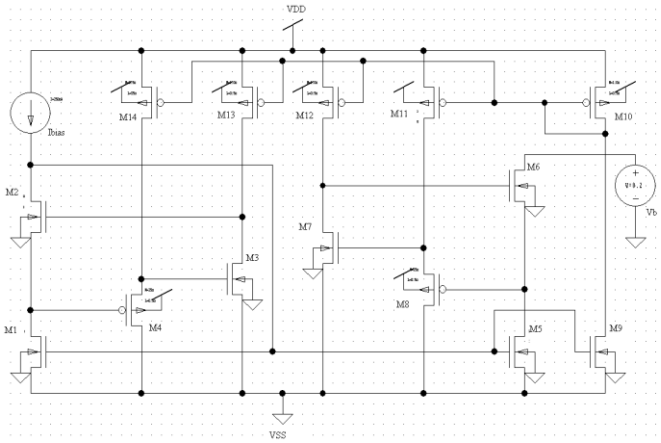

Figure 11: Wide output swing RCCM (WOS-RCCM)

VII. WIDE INPUT OUTPUT SWING REGULATED CURRENT MIRROR

The schematic of the proposed low voltage wide swing regulated cascode current mirror is shown in figure 12 the input current (*Iin*) is pumped into the drain of M1. As mentioned earlier, the bias current of M6 is kept small to operate it in sub-threshold region and M1 in saturation region. The transconductance (*gm*1) and channel conductance (*go*1) of M1 decides the input impedance (*Rin*). M6 provides the necessary gate drive to M1 and M2 and to M7 for adaptive biasing [11]. PMOSTs are used for shifting the dc level at the drains of input (M1) and output (M2) transistors, the level shifter will remain invisible for ac signal.

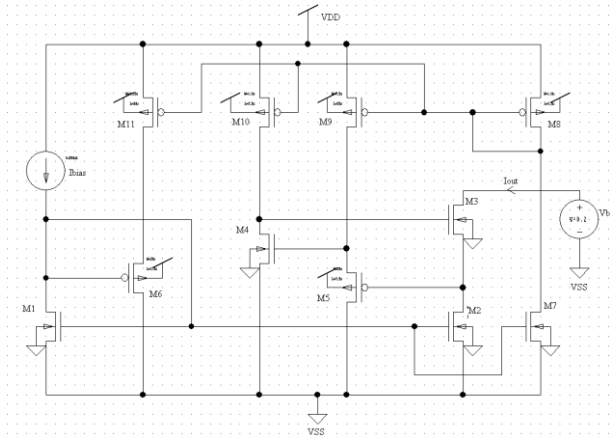

Figure 12: Wide Input-Output Swing Regulated Cascode Current Mirror

VIII. SIMULATION RESULT

C. Input Characteristics of Cascode Current Mirror

Figure 13 shows the input characteristics of cascode current mirror. Input voltage (Vin) is plotted by sweeping input current from 0 µA to 5 mA by using 0.18µm IBM MOS technology model parameters.

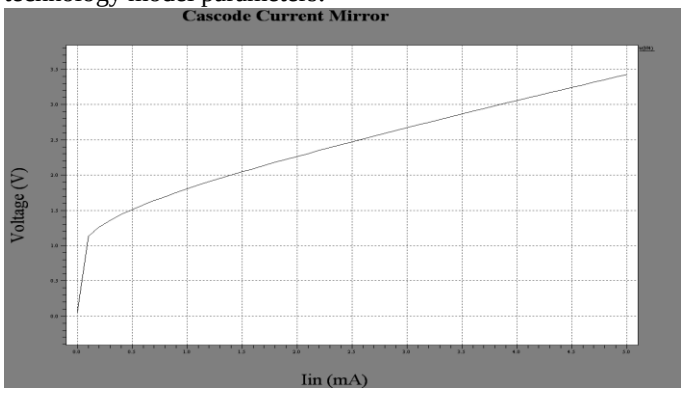

Figure 13: Input Characteristics of Cascode Current Mirror

B. Current Transfer Characteristics of Cascode Current Mirror

Figure 14 shows current transfer characteristics of cascode current mirror for 0.18µm IBM MOS technology parameters. Drain current id (M3) of transistor M3 is input or reference current and drain current id(M4) of transistor M4 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current.

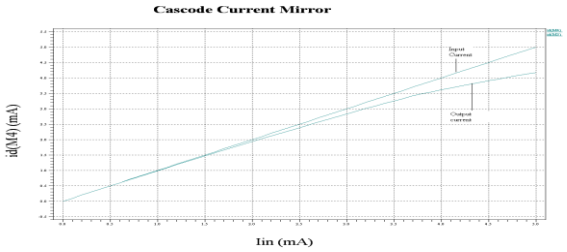

Figure 14: Current transfer characteristics of cascode current mirror

C.Input Characteristics of Low Voltage CMOS Cascode CM

The circuit shown in figure 15 is simulated using 0.18µm IBM model parameters with supply voltage of 1V. The purpose was to obtain a high performance LVCM that have high input and output voltage swing capabilities. Table 4.1 summarizes the (*W/L*) ratios of MOSFETs used in circuits. In figure 4.8 V_{in} is input voltage and I_{in} is input current and shows input voltage (V_{in}) requirement for various values of input current I_{In} . V_{in} Required is 0.51V for low voltage cascode current mirror structures at I_{out} of 1mA.

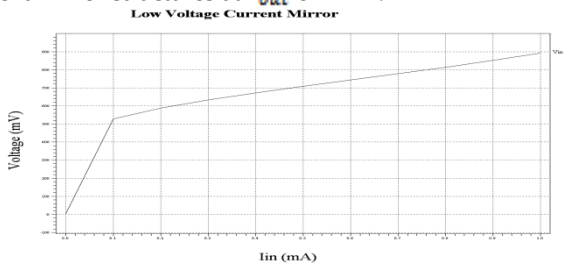

Figure 15: Input characteristics LVCM

D. Current Transfer characteristics of Low Voltage Current Mirror

Figure 16 shows current transfer characteristics of low voltage current mirror for 0.18µm IBM MOS technology parameters. Drain current id (M3) of transistor M3 is input or reference current and drain current id(M4) of transistor M4 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current.

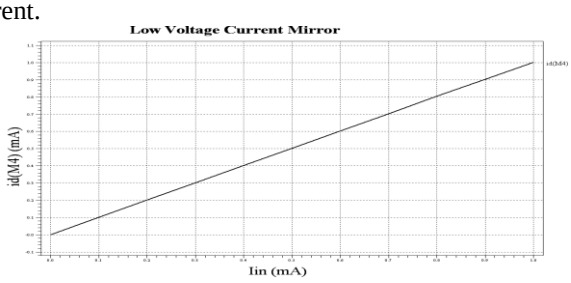

Figure 16: Current transfer characteristics LVCM

E.Power Dissipation Results for Low voltage Current Mirrror

Low voltage current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 1000µA. Width and length of transistors (M3 & M4 and M1 & M2) are kept same. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 17 shows power dissipation results. Power results are reported at the end of transient simulation in the output file

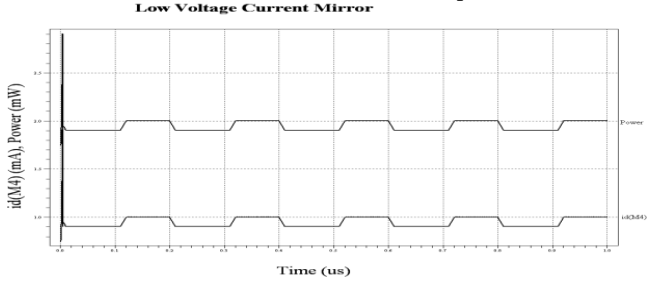

Figure 17: Power dissipation of LVCM

F. Frequency Response of Low Voltage Current Mirror

The frequency response of low voltage current mirror is shown in figure18. The frequency response of cascode current mirror is dependent on the capacitive load (Cload). In figure 4.11 the -3db banwidth is 240Mhz for a load capacitance of 10 pF.

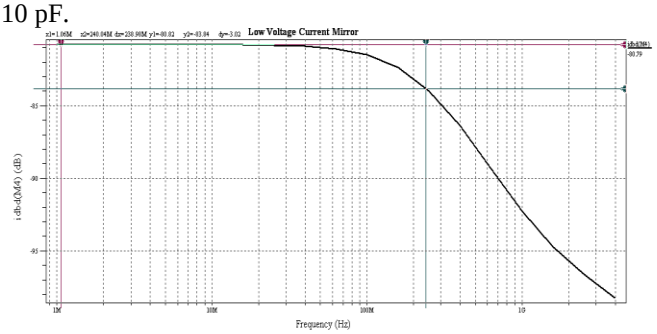

Figure 18: Bandwidth of Low Voltage Current Mirror

Aspect ratio of transistors used in low voltage current mirror is given in table I

Table I: Aspect Ratio of transistors used in LVCM current mirror

MOSFETs	Type	Width	Length
M1,M2,M3, M4	NMOS	20µm	0.5µm
M5	PMOS	10µm	0.3µm

Table II: Parameters used in Low Voltage Current Mirror (LVCM)

Parameter	Unit
Supply voltage	1.0 volt
V_{bias} (Voltage bias)	-0.2 volt
Threshold voltage V_{tn} (NMOS)	0.44 Volt
Transconductance	156.8µA

G. **Simulation Results & Waveforms of Regulated Cascode Current Mirror**

The circuits have been simulated using IBM, 0.18µm, parameters with supply voltage of 1V. The purpose was to obtain a high performance LVCM that have high input and output voltage swing capabilities. Table III summarizes the (*W/L*) ratios of MOSFETs used in circuits.

Table III: Transistors Aspect Ratios

Device	RCCM W/L Ratio	WOS – RCCM W/L Ratio	WIOS – RCCM W/L Ratio
M1,M2	25/0.5 NMOS	25/0.5 NMOS	25/0.5 NMOS
M3	0.5/0.5 NMOS	0.5/0.5 NMOS	25/0.5 NMOS
M4	25/0.5 NMOS	25/0.5 PMOS	0.5/0.5 NMOS
M5	25/0.5 NMOS	25/0.5 NMOS	25/0.5 PMOS
M6	0.5/0.5 NMOS	25/0.5 NMOS	25/0.5 PMOS
M7	1.0/0.5 NMOS	0.5/0.5 NMOS	1.0/0.5NMOS
M8	1.0/0.5 PMOS	25/0.5 PMOS	1.0/0.5 PMOS

M9	1.0/0.5 PMOS	1.0/0.5 NMOS	0.5/.25 PMOS
M10	1.0/0.5 PMOS	1.0/0.5 PMOS	1.0/0.5 PMOS
M11	-	0.5/0.5 PMOS	0.25/.88 PMOS
M12, M13	-	1.0/0.5 **PMOS**	-
M14	-	0.5/0.25 **PMOS**	-

H. Input Characteristics (Input signal swing) of Regulated Cascode Current

Figure 4.21 shows the input characteristics of regulated cascode current mirror as shown in figure 19. Input voltage (Vin) is plotted by sweeping input current from 0 µA to 250 µA by using 0.18µm IBM MOS technology model parameters. In figure 4.21 Vin is input voltage and Ibias is input current and shows input voltage (V_{in}) requirement for various values of input current I_{In}. V_{in} required is 0.49V for Regulated Cascode Current Mirror structures at I_{out} of 200µA.

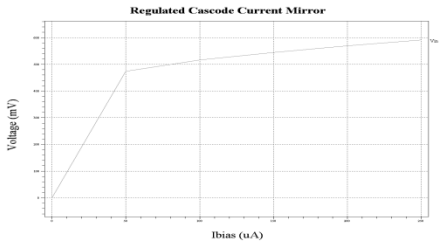

Figure 19: Input characteristics Regulated Cascode Current Mirror

I. Current Transfer Characteristics of Regulated Cascode Current Mirror

Figure 20 shows current transfer characteristics of regulated cascode current mirror for 0.18µm IBM MOS technology parameters. Drain current id (M2) of transistor M2 is input or reference current (Ibias) and drain current id(M5) of transistor M5 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current. output current very from 1µA to 1mA. We find that current transfer ratio $(I_{out}/I_{in})$is almost 1 for input current range of 30nA to 220µA (error < ±0.3%).

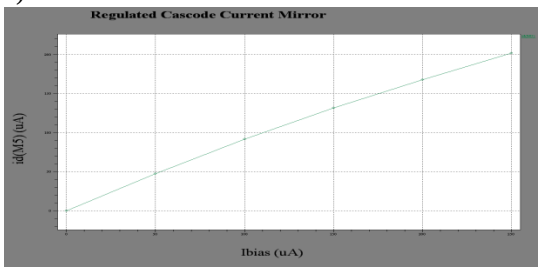

Figure 20: Current transfer characteristics RCCM

J. Power dissipation result for Regulated Cascode Current Mirrror for 0.18µm technology

Regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 1mA. Width and length of transistors (M3 & M4 and M1 & M2) are given in table III. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 21 shows power dissipation results. Power results are reported at the end of transient simulation in the output file.

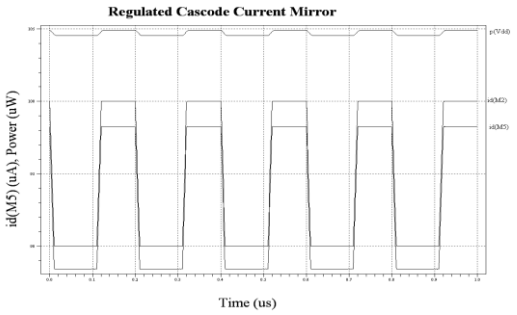

Figure 21: Power dissipation of RCCM

K.Output characteristics of Regulated Cascode Current Mirror at High Currents

Regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V. Figure 22 shows the output current characteristics at high current at different – different input current value and input current 0µA to 200µA.

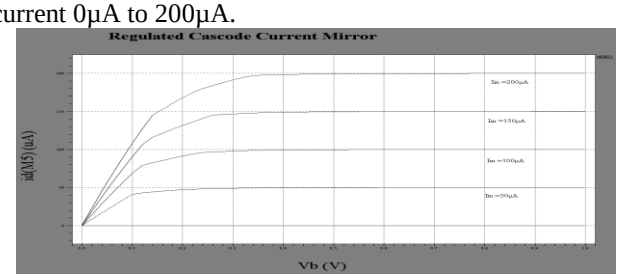

Figure 22: Output Current Characteristics at High Currents

L.Output characteristics of Regulated Cascode Current Mirror at Low Currents

Regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V. Figure 23 shows the output current characteristics at low current at different – different low input current value andcurrent 0nA to 200nA..

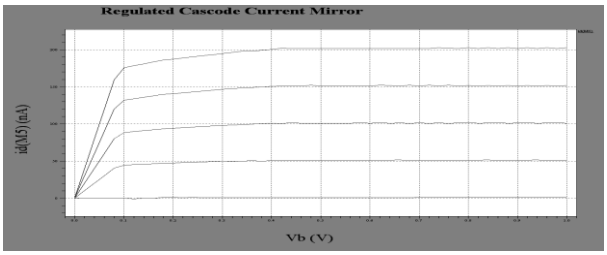

Figure 23: Output Current Characteristics at Low Currents

M. Simulation Results & Waveforms of Wide Output Swing Regulated Cascode Current Mirror

Input Characteristics of WOS –RCCM

input characteristics of wide output swing regulated cascode current mirror as shown in figure 24. Input voltage (Vin) is plotted by sweeping input current from 0 µA to 250 µA by using 0.18µm IBM MOS technology model parameters. In figure 4.26 Vin is input voltage and Ibias is input current and shows input voltage (V_{in}) requirement for various values of input current I_{In}. V_{in} Required is 0.49V for wide output swing regulated cascode current mirror structures at I_{out} of 200µA

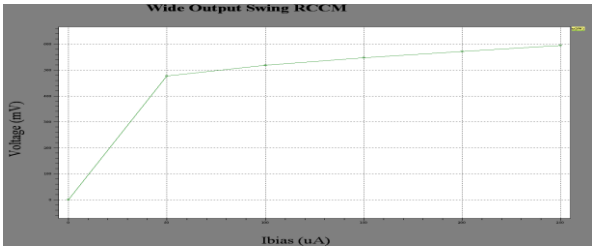

Figure 24: Input characteristics Wide Output Swing RCCM

N.Current Transfer Characteristics of Wide Output Swing Regulated Cascode Current Mirror

Figure 25 shows transfer characteristics of wide output swing regulated cascode Current Mirror for 0.18µm IBM MOS technology parameters. Drain current id (M2) of transistor M2 is input or reference current (Ibias) and drain current id(M6) of transistor M6 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current. We find that current transfer ratio $(I_{out}/I_{in})$is almost 1 for input current range of 30nA to 220µA (error < ±0.4%).

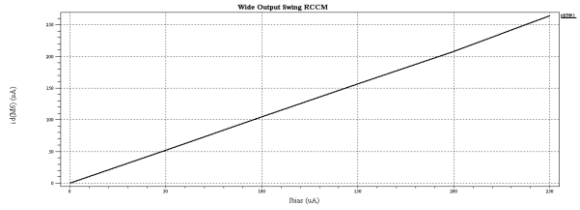

Figure 25: Current Transfer characteristics Wide Output Swing RCCM

O. Output Current Transfer characteristics at High currents wide swing RCCM

Wide swing regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V. Figure 26 shows the output current characteristics at low current at different – different low input current value.

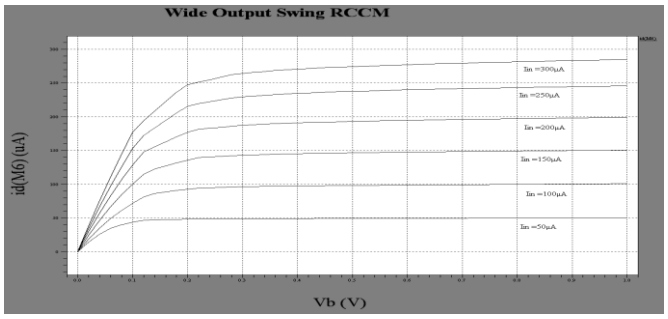

Figure 26: Output Current Transfer characteristics at High currents

P. Output Current Transfer characteristics at low currents of wide swing RCCM

Wide swing regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V. Figure 27 shows the output current characteristics at low current at different – different low input current value.

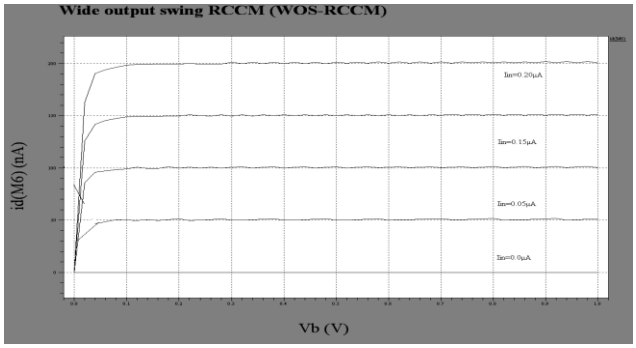

Figure 27: Output Current Transfer Characteristics at Low Currents

Q. Output signal swing wide output swing regulated cascode current mirror

Wide output swing regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and Iin 100µA. It is seen that wide output swing RCCM saturated Vb = 0.17V.

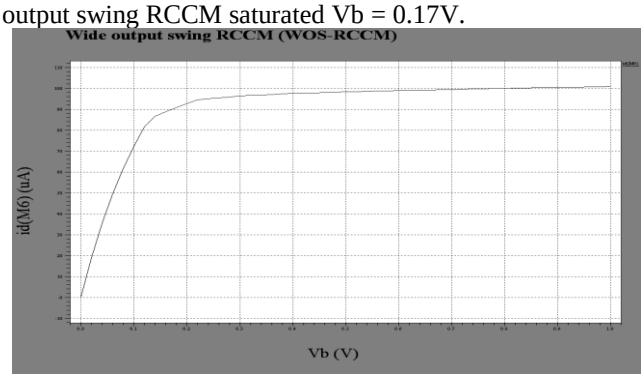

Figure 28: Output signal swing WO–RCCM

R. Power dissipation result for wide output swing regulated cascode current mirrror

Wide output swing regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 100µA. Width and length of transistors (M3 & M4 and M1 & M2..M14) are given in III. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 29 shows power dissipation results. Power results are reported at the end of transient simulation in the output file.

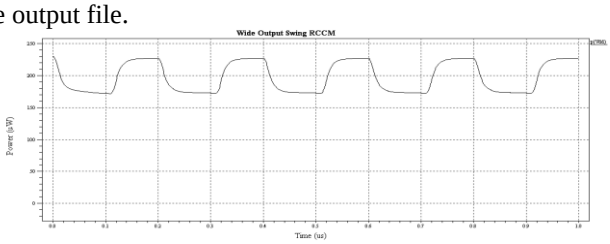

Figure 29: Power dissipation of WOS-RCCM

S. Simulation Results & Waveforms of Wide Input Output Swing Regulated Cascode Current Mirror

S.1 Input Characteristics of WIOS-RCCM

Figure 4.32 shows the input characteristics of wide input output swing regulated cascode current mirror as shown in figure 30 Input voltage (Vin) is plotted by sweeping input current from 0 µA to 250 µA by using 0.18µm IBM MOS technology model parameters.

In Figure 4.32 Vin is input voltage and Ibias is input current and shows input voltage (V_{in}) requirement for various values of input current I_{in}. V_{in} required is 0.34V for wide output swing regulated cascode current mirror structures at I_{out} of 200µA.

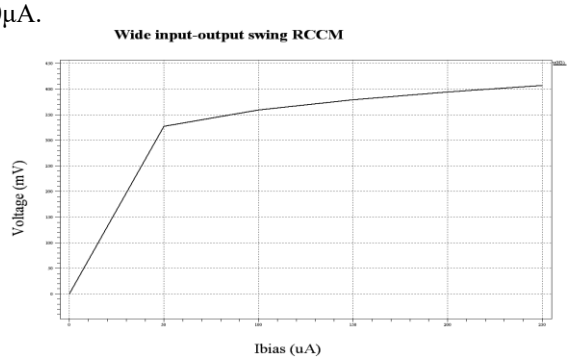

Figure 30: Input characteristics Wide Input Output Swing RCCM

S.2 Current Transfer Characteristics of WIOS-RCCM

Figure 31 shows transfer characteristics of wide input output swing regulated cascode Current Mirror for 0.18µm IBM MOS technology parameters. Drain current id (M1) of transistor M1 is input or reference current (Ibias) and drain current id(M3) of transistor M3 is the output current. From simulated waveform, it is very clear that output current very closely tracks the input or reference current. We find that current transfer ratio $(I_{out}/I_{in})$is almost 1 for input current range of 30nA to 220µA (error < ±0.4%).

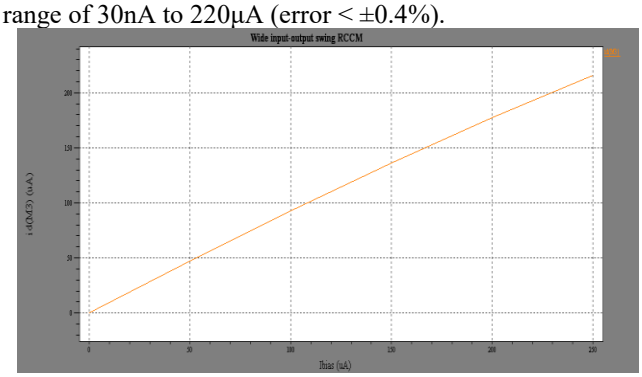

Figure 31: Current Transfer Characteristics WIOS-RCCM

S.3 Output Voltage Swing Characteristics WIOS-RCCM
Figure 32 shows output characteristics of wide input output swing regulated cascode Current Mirror for 0.18µm IBM MOS technology parameters. Here WIOS- RCCM wider output signal and input signal swing.

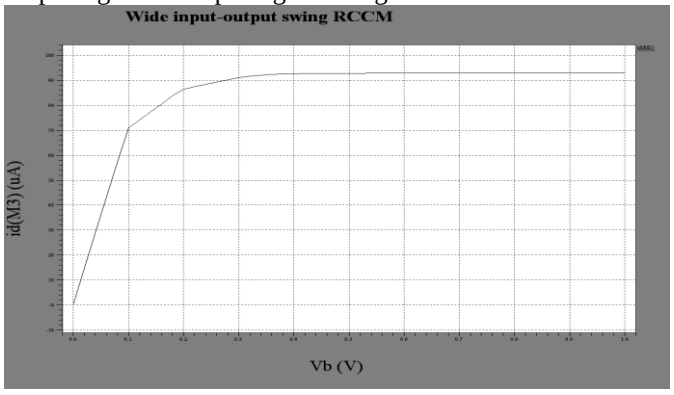

Figure32: Output Voltage Characteristics WIOS-RCCM

S..4 Output Characteristic at High Current of WIO-RCCM

At zero I_{in} (thus V_{tn} is also zero), the input level shifter (M6) in the WIOS-RCCM structure solely decides V_{gs2} to be near V_{tn} since, V_{ds2} increases independently with bias voltage Vb, therefore M2 conducts in sub-threshold region, and a small current called offset current (*Ioffset*) flows through it. Figure 33 shows output characteristics of WIOS-RCCM. The CM structure offers negligible amount of I_{offset}. Figure shows 4.35 the characteristics high biasing voltage Vb verses output current.

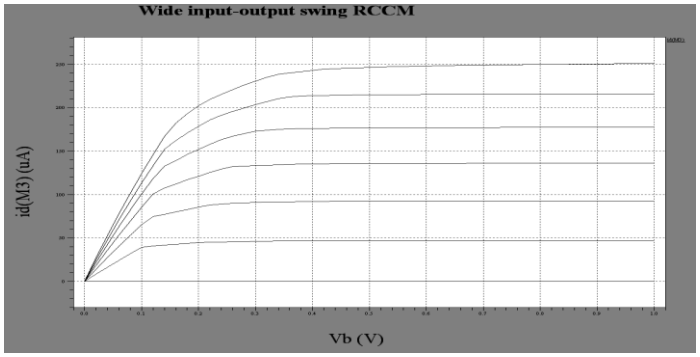

Figure 33: output Characteristics at high currents WIOS-RCCM

S.5 Output Current Transfer characteristics at low currents of WIOS-RCCM

Wide input output swing regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V.Figure 34 shows the output current characteristics at low current at different – different low input current value.

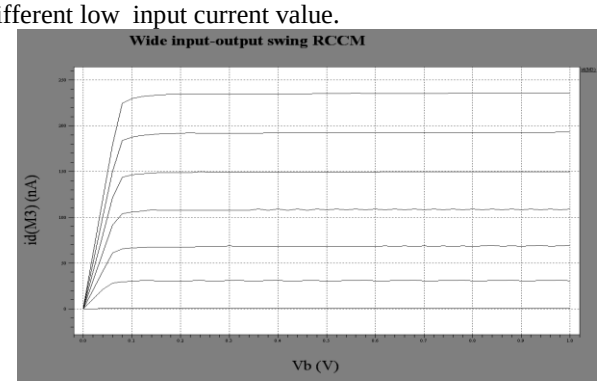

Figure 34: Output Characteristics at Low currents

S.6 Power dissipation result forWIOS -Regulated Cascode Current Mirrror

Wide Input Output Swing Regulated cascode current mirror circuit is simulated using 0.18µm IBM MOS model parameters with supply voltage 1.0 V and I_{in} of 100µA. Width and length of transistors (M3 , M4 , M1 , M2 …. M11) are given in table III. Transient analysis is used to calculate the power dissipation in the current mirror. Figure 4.38 shows power dissipation results. Power results are reported at the end of transient simulation in the output file.

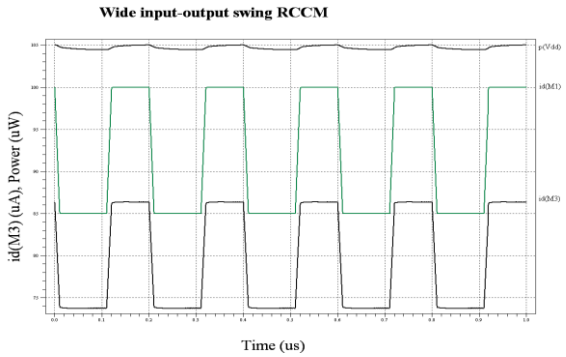

Figure 35: Power dissipation of WIOS –RCCM

IX. COMPARISON

A. Comparison of Power Dissipation of RCCM, WOS-RCCM and WIOS-RCCM

The comparison of power dissipation of present work i.e. current mirror architectures of RCCM, WOS RCCM, WIOS-RCCM with the reference works [7] as shown in figure 36. Reference work was done in 0.25µm technology and the present work is done in 0.18µm IBM MOS technology. Figure 36 shows the improvement in each architecture as compared to the reference work in terms of power dissipation.

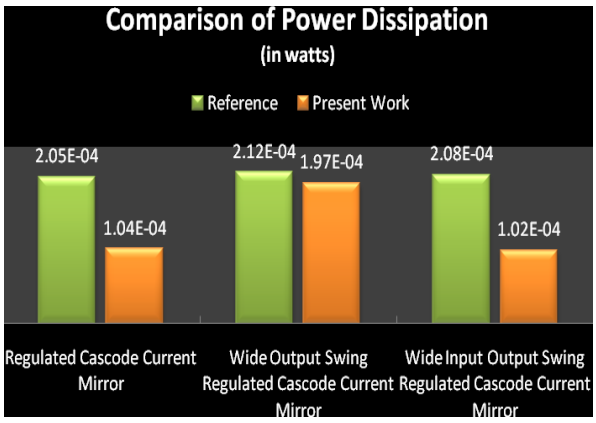

Figure 36. Comparison of Power dissipation of RCCM

B. Comparison of Input voltage swing Capability of RCCM, WOS-RCCM and WIOS-RCCM

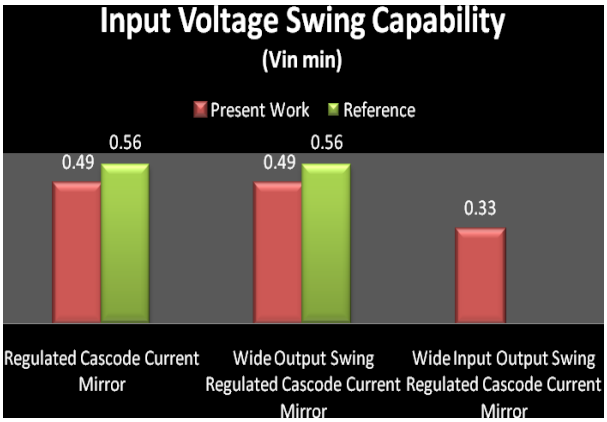

Figure 37. Comparison of Input voltage swing capability

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