A Study Single Electron Transistor in Neural Network, Nanotechnology and Memory Design

Shivani Chauhan

Abstract— To avail the practical approach for low dimension designing of electronic chips , SET is being used on the highest concern to provide nanotechnology . Now in current days , artificial neural networks is playing important roll for the accuracy and less time response . A computer memory which is basically based on this property would be ability to retain information in case if processor it self powered off . SET is to be considered as elements for future low power , high density integrated circuits reason for this of their the potential to involving only few electrons for ultra low power . In this paper we express the study of single electron transistor being used in nanotechnology , artificial neural network & memory designing . the operation as single electron transistor with it's history is mentioned included with advantages and disadvantage of SET .

Index Terms— Operation of set , Nanotechnology , Neural Network & Current Standards.

I. INTRODUCTION

The scaling down of the size of MOSFETs has been the basic of the semiconductor industry for the last 30 years. Metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the most prevalent electron devices for ULSI applications, and by which the scaling down of the sizes of MOSFETs [1][2] has been the basis of the development. The single-electron transistor (SET) is basically a three-terminal device, which electric characteristics of which are governed by the movement of single electrons. The SET's physical size is comparatively very small and its performance, such like ON-OFF current ratio, improves as its size is reduced. SET is being used in artificial neural networks for accurate and fast results . Nanotechnology operates at the first level of organization of atoms & molecules for both living and anthropogenic systems. This is place where the properties and functions of all systems are defined .nano technology is a key component . According to the various research reports the transistor's central component is an island of only 1.5 nanometers in diameters and is being operated with only a or two electron it's state is assumed to sensitivity at small pressure changes at nanoscale , to make such a device potentially useful for nanoscale charge and force sensor . A computer memory which is basically based on this property would be ability to retain information in case if processor it self powered off . SET is to be considered as elements for future low power , high density integrated circuits reason for this of their the potential to involving only few electrons for ultra low power . to make practically it useful however , Single Electron Transistor must be operate at room temperature . thermal fluctuation limitation and capacitance requires that the size of island of SET not to exceed over 10 nm , a conventional size out of the range to present conventional process of micro fabrication for the operation of single electron on room temperature memory is being realized to use of self organized , small size over thin poly silicon films.

II. SET OPERATION

Scaling down of electronic device sizes has been the fundamental strategy for improving the performance of ultra-large-scale integrated circuits (ULSIs). Metal-oxide-semiconductor field-effect transistors (MOSFETs) have been the most prevalent electron devices like for ULSI applications, and thus the scaling low of the sizes of MOSFETs [1][2] has been the basis of the development of the semiconductor industry for the last 30 years. However, in the early years of the 21st century, the scaling of CMOSFETs is entering the deep sub-50 nm regime [3]. In this deep nanoscaled regime, fundamental limits of CMOSFETs and technological challenges with regard to the scaling of CMOSFETs are encountered [4]. On the other hand, quantum-mechanical effects are expected to be effective in these small structured devices by which Therefore, in order to increase the prodigious progress of LSI performance in single electron transistor, it is essential to introduce a new device having an operation principle that is effective in smaller dimensions and which may achieve and access the quantum- mechanical effects, and by which they thus provide a new functionality beyond that attainable with CMOSFETs. Electrons are transferred single by single using coulomb blockodes effect in a set of three terminal device . the principal of operation is based upon the fully controlled flow of charge from and to island via two tunneling junctions.

III. HISTORY OF SINGLE ELECTRON TRANSISTOR

Single-electron transistor (SET) is very popular in the field of nanoelectronics since a decade. Single electron transistor (SET) is the most fundamental three-terminal single electron device (SED) which is capable of offering low power consumption and high Operating speed.

Manuscript received April 11, 2013.
Ms Shiwani chauhan, Department of ECE, KIIT College Of Engineering, Sohna Road, Gurgaon, India.

*Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication*

Since the technology reaches nanoscale size, the behavior of a nanoelectronic single electron transistor (SET) is controlled by the quantum mechanical appeared effects.

IV. APPLICATION OF SET

A. Supersensitive Electrometer

The single-electron transistors has a high sensitivity witch enabled them as electrometers in unique physical experiments. They have designed possible unambiguous observation of parity effects in various superconductors , for example only . to measure the absolute value of extreme low dc current have been demonstrated . To proof the existence of fractional charge excitation in hall effect fractional quantum a updated version of transistor is used [14]. Which is also used in the first measurements of single-electron effects in single-electron traps and boxes.

B. Single-Electron Spectroscopy

Out of various important applications of single –electron transistor the most important one is the possibility of measuring the energies of additional electrons by which energy level is distributed in nanosacale objects specially quantum dots [15].

C. DC Current Standards

One of the possible applications of single-electron transistor tunneling is basics standards of dc current Bloch oscillations in a simple oscillator or for such a standard a phase lock SET oscillations with a well characterize frequency f in an external rf source . the transfer of a certain number of electrons per period which is provided by The phased locked of external rf signal . by which the generation of dc current takes place and which is fundamentally related to frequency as $I = mef$. Such type of arrangement have limitation of coherent oscillation that are which do not exhibit coherent oscillations in the autonomous mode. Later overcome by the use of such a stable rf source to drive devices such as single-electron turnstiles and pumps.

D. Temperature Standards

The absolute temperature can be developed by the use of 1D single-electron arrays One new avenue toward a new standard of . Arrays with N>>1 islands exhibit dc I-V curves generally equal to those of capacitance at low voltages ($|V| < V_t$) and approaching the linear asymptote V = NRI + const at ($|V| \gg V_t$) and the IV curve is almost linear at all voltages:$G \equiv {}^{dI}/_{dV} \approx G_n \equiv {}^{1}/_{NR}$ If the temperature is raised and single-electron transistors with a clear Coulomb blockade of tunneling at low temperatures . Above E_c/k_B, thermal fluctuations smear out the Coulomb blockade, . The only remaining artifact of the Coulomb blockade is a low dip in the various individual conductance around V=0 [19]

E. Detection of Infrared Radiation

To electromagnetic radiation the photo response of single-electron systems with frequency $f \approx E_c/h$ which have shown that generally the response varies accordingly from that the well-known Tien-Gordon theorem of photon-assisted tunneling. In fact, this is basically based on the various assumption that the tunneling events are uncorrelated, while in single-electron systems the additional electron transfer is typically correlated. This fact shows that single-electron devices, especially 1D multi-joint array with their low co-tunneling rate, is being used for ultrasensitive video- and heterodyne detection of high frequency electromagnetic radiation, equally as to the superconductor-insulator-superconductor (SIS) arrays and junctions . The Single electron array have advantages over their SIS counterparts: Firstly lower shot noise and secondly convenient valence conjunction of the threshold voltage. Where no background-radiation-limited detectors are yet available this opportunity is especially promising for detection in the few-terahertz frequency band region, [19].

F. Voltage State Logics

In case of voltage state single electron transistor can be used . in such a mode , the input gate voltage U controls the source-drain current of the single electron transistor which is being used in digital logic circuits, closely and equally to the usual field-effect transistors (FETs). This refers that the single-electron charging effects are confined to the interior of the transistor, on other hand while externally it similar to the usual electronic device switching multi-electron currents, with binary unity/zero presented with up/down dc voltage levels (physically not quantized). This concept simplifies that for relatively large devices operating at helium temperatures. At the prospective room-temperature, however operation which may or may not ignore all the single-electron physics particulars this power becomes on the order the circuit design. One disadvantage of voltage state circuits is that of the transistors in each complementary pair is closed too well, so that the leakage current statically in these circuits is fairly substantial, of the order of 10^{-4} e/RC. Power consumption The corresponding statically is negligible of 10^{-7} Watt per transistor. Though apparently low, this number provides an unacceptable static power dissipation density (>10 kW/cm^2) for the hypothetical circuits which may be dense enough (>1011 transistors per cm2) to create regular a real challenge for the prospective CMOS technology [16].

G. Charge State Logics

by using of charge state logic the main problem of leakage current is solved in which only a bit of information are presented by the absence /presence of single electrons at certain conducting islands throughout the whole circuit. the static currents and power vanish these circuits since so there is no dc current in any static state.

V. DISADVANTAGE OF SET

The main problem with all the known types of single-electron logic is devices in the requirement which in practice means sub nanometer island size for room temperature operation .To handle SETS at room temperature, very large quantities of monodispersed Nan parts which is less than 10nm in diameter should be synthesized. it is not easy to construct v large quantities of SETs by traditional semiconducting process and optical lithography.

It is difficult to link SETs with the which is practically difficult to construct and fabricate Single electron transistors (SETs).

VI. ADVANTAGE OF SET

- High sensitivity
- Simplified circuit
- Feature of reproducibility
- Straight forward co-integration with traditional CMOS circuits
- Performance of Single-electron transistors (SETs) is much higher than the Field-effect transistors (FETs) because of their small size.
- Simple principle of operation
- Compact size
- Single electron transistors (SETs) contains low voltage gain and high input impedances . Besides this, these are also very sensitive to random and additional background charges. Because of this , SETs have replaced the FETs in many applications where it is required to achieve large voltage gain is necessary and low output impedances .
- Low energy consumption

High operating speed .

VII. SET IN NANOTECHNOLOGY

According to the various research reports the transistor's central component is an island of only 1.5 nanometers in diameters and is being operated with only a or two electron . that capability would be the important transistor to a wide range of computational application , from ultra dense memories to quantum processors the all powerful devices which promise to crack the issue so complex like all of the computer's being operated together for billions of years not break them , the electronic devices like wires and transistor of nanoscale dimensions at the interface of a crystal of strontium titan ate & a 1.2 nanometer thick layer of lanthanum aluminates . the electronic devices can be interface used anew and erased accordingly . the first single-electron transistors made entirely of oxide-based materials ,the sketch SET contain of an island formation which can house up to two electrons . the no of electron in both matter either increased or decreased varies in distinct conductive properties .To carry a additional electron across the island the extending wires is use . the SET is extremely sensitive to any electric charges , which is a basic virtue of SET. ferroelecrticity which is a great extended property among them , which permits transistor to act like solid state memory . In the absence of external power , ferroelectric state can control over island in matter of number of electrons which generally display two sates of memory element 1 or 0 . it's state is assumed to sensitivity at small pressure changes at nanoscale , to make such a device potentially usefull for nanoscale charge and force sensor . A computer memory which is basically based on this property would be ability to retain information in case if processor it self powered off.

VIII. SET IN ARTIFICIAL NEURAL NETWORK

SET is being used in artificial neural networks for accurate and fast result . it is possible to make artificial neural network with very low power characteristics and power , with respect to SET technology . the most attractive candidates of Single Electron Transistor nano scale devices for CMOS very large scale integrated chips era basically due to very low power consumption . the latching of nanoscale switches is baeds on controlled SET and trapping is served as synaptic basis for highest dense and very high selg evolving binary weight , analog signal neural network .

IX. SET IN MEMORY DESIGNING

SET is to be considered as elements for future low power , high density integrated circuits reason for this of their the potential to involving only few electrons for ultra low power . to make practically it useful however , Single Electron Transistor must be operate at room temperature . thermal fluctuation limitation and capacitance requires that the size of island of SET not to exceed over 10 nm , a conventional size ourt of the range to present conventional process of micro fabrication for the operation of single electron on room temperature memory is being relized to use of self organized , small size over thin poly silicon films . it's not easy to restrict the structure and size of SET island with spontaneous size formation method of fabrication . A SET memory with metal –oxide semiconductor FET is being fabricated in silicon –on-insulator material for sensing . Single Electron Transistor , is bounded to a memory node , which is expressed in the silicon layer . the metal oxide semiconductor FET which can be formed memory node with it's channel is substrate silicon . There are 2 individual states of the memory node voltage at 4.2 K , which is separated by coulomb gap Single Electron Transistor . Field effect transistor metal oxide semiconductor current shows the proof of gate dependent oscillation by conductance in two SET

X. CONCLUSION

A computer memory which is basically based on this property would be ability to retain information in case if processor it self powered off . In nanoelectronics the single electronic devices are very promising posses various characteristics that can explore new applications and can fuel the technology development in different fields like memory, radiation detection, switching logics etc. thus through the study of SET operation in the island electron controlled process and the application of the single electron transistor in neural network . one bit memory application is a process where single electron transistor is highly used . thus through the application of SET we reached to a approach for the various use of sigle electron transistor in memory , neural network and nanotechnology .

REFERENCES

1. M.A. Kastner, "*The single Electron Transistor*", Reviews of Modern Physics, Vol. 64, No. 3, pp. 849-858, July 1992.
2. M. A. Kastner, "*The single electron transistor and artificial atoms*", Ann. Phy. (Leipzig), vol. 9, pp. 885-895, 2000.

3. S. Bednarek, B. Szafran, and J. Adamowski, "*Solution of the Poisson-Schrodinger problem for a single-electron transistor*", Phys. Rev. B, Vol. 61, pp. 4461-4464, 2000.
4. Songphol Kanjanachuchai and Somsak Panyakeow, "*Beyond CMOS: Single-Electron Transistors*", IEEE International Conference on Industrial Technology, Bangkok, Thailand, 2002.
5. Masumi Saitoh, Hidehiro Harata1ion and Toshiro Hiramoto, "*Room-Temperature Demonstration of Integrated Silicon Single-Electron Transistor Circuits for Current Switching and Analog Pattern Matching*", IEEE International Electron Device Meeting, San Francisco, USA, 2004.
6. K. Matsumoto, M. Ishii, K. Segawa, Y. Oka B. J. Vartanian and J. S. Harris, "*Room temperature operation of a single electron transistor made by the scanning tunneling microscope nano oxidation process for the TiOx/Ti system*", Appl. Phys. Lett. 68 (1), pp. 34-36, 1996.
7. Xiaohui Wang and Wolfgang Porod, "*Analytic I-V Modeling for Single-Electron Transistor*", VLSI Design, Volume 13, pp. 189-192, 2001.
8. J.M. Martinez-Duart, R.J. Martin-Palma, F. Agullo-Rueda, "*Nanotechnology for Microelectronics and Optoelectronics*", First Edition, pp.65-169, 2006.
9. William a. Goddard, Donald W. Brenner, Sergey e. Lyshevski, Gerald J. Lafrate, "*Handbook of Nanoscience Engineering and Technology*", Second edition, pp.13-1 to 13-38, 2007.
10. Uda Hashim and Amiza Rasmi "*Single- Electron Transistor (SET) Process and Device Simulation Using SYSNOPSYS TCAD Tools*" American Journal of Applied Sciences 3 (7): 1933-1938, 2006
11. T.A. Fulton and G.D. Dolan, "*Observation of single-electron charging effect in small tunneling junction*," Phys. Rev. Lett., vol.59, pp. 109-112, July 1987.
12. Dae Hwan Kim, Jong Duk Lee and Byung-Gook Park "*Room Temperature Coulomb Oscillation of a Single Electron Switch with an Electrically Formed Quantum Dot and Its Modeling*", Jpn. J. Appl. Phys. Vol. 39 (2000) pp. 2329-2333, April 2000.
13. Dinh Sy Hien, Huynh Lam Thu Thao and Le Hoang Minh, "*Modelling transport in single electron transistor*", APCTP–ASEAN Workshop on Advanced Materials Science and Nanotechnology (AMSN08), Journal of Physics: Conference Series 187,pp. 1-5, 2009.
14. David Berman, Nikolai B. Zhitenev, Raymond C. Ashoori, Henry I. Smitha and Michael R. Melloch, "*Single-electron transistor as a charge sensor for semiconductor applications*", J. Vac. Sci. Technol. B 15(6), pp. 2844-2847, Nov/Dec 1997.
15. M. N. Kiselev, K. Kikoin, R. I. Shekhter and V. M. Vinokur, "*Kondo shuttling in a nanoelectromechanical single-electron transistor*", PHYSICAL REVIEW B 74, 233403, pp. 1-4, 2006.
16. Lingjie Guo, Effendi Leobandung and Stephen Y. Chou, "*A Silicon Single-Electron Transistor Memory Operating at Room Temperature*", SCIENCE VOL. 275, pp. 649-651, 1997.
17. Dong Seup Lee, Sangwoo Kang, Kwon-Chil Kang, Joung-Eob Lee, Jung Hoon Lee, Kwan-Jae Song, Dong Myong Kim, Jong Duk Lee and Byung-Gook Park, "*Fabrication and Characteristics of Self-Aligned Dual-Gate Single-Electron Transistors*", IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 8, NO. 4, pp. 492-497, JULY 2009.
18. Changyun Zhu, Zhenyu (Peter) Gu, Li Shang, Robert P. Dick and Robert G. Knobel, "*Towards An Ultra-Low-Power Architecture Using Single-Electron Tunneling Transistors*", Annual ACM IEEE Design Automation Conference, pp. 312-317, 2007.
19. Teruhisa Matsui, Jun Kawarabayashi, Kenichi Watanabe and Tetsuo Iguchi, "*Evaluation of Single-Electron Transistor as Nanoscale Thermometer for a Cryogenic Radiation Detector*", Journal of NUCLEAR SCIENCE and TECHNOLOGY, Supplement 6, pp. 73–77 September 2008.
20. R. Knobel, C. S. Yung, and A. N. Clelanda, "*Single-electron transistor as a radio-frequency mixer*", APPLIED PHYSICS LETTERS, VOLUME 81, NUMBER 3, pp. 532-534, July 2002.
21. A.N. Cleand, D. Estene, C. Urbina and M.H. Devoret, "*An Exterimly Low Noise Photodetector*
22. [Om kumar and Manjit kaur, "Single electron transistor: Applications & problems", International journal of VLSI design and communication system (VLSICS) Vol. 1, No. 4, Dec. 2010.

AUTHORS PROFILE

Ms. Shivani chauhan is a student of M.tech final year under the Department of Electronics and Communication Engineering from KIIT College Of Engineeing, Sohna Road Gurgaon . Her area of interest is analog design.