Hybrid Topologies of Multilevel Converter for Current Waveform Improvement

N. Susheela, P.Satish Kumar, B.Sirisha

Abstract— This paper presents different multilevel converter topologies that includes NPC, NPC-CHB, FC, FC-CHB converter. The operating principle of each topology and a review of the most relevant modulation methods are discussed. Multilevel converters offer advantages in terms of the output waveform quality due to the increased number of levels used in the output voltage modulation. This advantage is particularly true for cascade H-bridge (CHB) converters that can be built to produce a large number of levels owing to their modular structure. Nevertheless, this advantage comes at the cost of multiple dc links supplied by independent rectifiers through the use of a multi-output transformer for inverters. This front end complicates the implementation of converters that have a high number of levels. An alternative method of using lower voltage cells with floating dc links to compensate only for the voltage distortion of a neutral-point-clamped and flying capacitor converter is considered for active rectifier applications. The analogy between the floating HBs and the series active filters is used to develop a strategy for the harmonic compensation of the NPC output voltage and the control of the floating dc-link voltages. This simplifies the current control scheme and increases its bandwidth. The proposed topologies have been verified using MATLAB/Simulink. The results show the improvement in the output current waveforms.

Index Terms—Current Control, dc link voltage, High-Power applications, Multilevel Converter

I. INTRODUCTION

In the last decade, medium-voltage high-power converters have become widely used as drives for pumps, fans and material transport in a number of industries, as well as for VAR compensation in grid applications [1], [2]. At this voltage range, multilevel converters are preferred to overcome the voltage blocking limitations of the available switches. This technology is also advantageous in improving output waveforms due, to the higher number of levels in the output voltage waveform, Along with a reduced input filter size for grid connected applications. Moreover, a high number of levels allow the device switching frequency to be reduced for a given current distortion.

Multilevel converters have been continuously developed in recent years due to the need to increase the power level in industry. The main reason for this is the capability of these topologies to handle voltage in the range of kilovolts and megawatts with medium-voltage semiconductors. The neutral-point-clamped (NPC) inverter presented in the early 1980s has become a standard topology for industrial applications.

However, as the number of output voltage levels increases, this topology presents some problems, mainly with the clamping diodes and the balance of the dc-link capacitors.

The multilevel topologies can be classified into three main categories: the neutral point clamped (NPC), the flying capacitors (FC) and the cascaded H-bridge (CHB) converters. The three level NPC Bridge is probably the most widely used topology for medium voltage AC motor drives and PWM active rectifiers. NPC converters with more levels are also possible, although there are significant problems in the balancing of their dc-link capacitor voltages, unless modified modulation strategies or additionally circuitry are used [3-7].

On the other hand, the CHB converter is normally implemented with large number of levels, but at the cost of complicated and bulky input transformers with multiple rectifiers or multi-winding three-phase output transformers. For this reason, in applications with no active power transfer, such as in reactive power compensation, where the converter can operate without the rectifier front-end, the CHB is a highly attractive solution [8-9].

An alternative for the NPC inverters are multicell topologies. The name “multicell” is derived from the fact that these inverters are based on the interconnection of modular structures generically called *cells*. Different cells, and different ways to interconnect them, generate many topologies [10-17]. The most important ones are namely, cascaded multicell (CM) and flying capacitor (FC). These topologies are easily scalable and present some benefits when they operate under internal fault states, due to the existence of redundant states. Based on those three basic topologies, many sub topologies and hybrid topologies, including their own modulation techniques, have been presented in the literature [18–21]. Different kinds of cells are used for a CM converter. In this way high-power low-switching-frequency cells are connected in series with lower power high-switching-frequency cells, generating high-quality voltage waveforms. In the same way, in [22-24] a high-power NPC converter is connected in series with floating H-bridge modules. Then, the active power is provided by the NPC, while the H-bridges are used to improve the output voltage waveforms by eliminating the low order harmonics generated by the NPC. A different approach is presented in [24], where two single-phase NPC legs are used to obtain a five-level cell for a CM cell. More complex topologies are presented in [25]–[27]. The HMC inverter achieves a higher number of output voltage levels with the same quantity of switches as equivalent converters while using a very simple modulation scheme.

Manuscript received March 15, 2013.

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It also presents lower losses since some of the semiconductors commutate at the output's fundamental frequency and, under the proposed modulation scheme, with zero voltage, thus allowing the use of slow turn on devices such as IGCT's or the safety series connection of IGBT's.

In recent years an increased interest has been given to hybrid topologies integrating more than one topology in a single converter. Several Hybrid topologies are proposed earlier. For Example cascaded H-bridges fed by multilevel dc-links generated which are implemented with another converter topology. In [24] a hybrid configuration based on the combination of an active NPC and a flying capacitor cell has been proposed to implement a five level converter. An hybrid converter formed by the series connection of a main three-level NPC converter and auxiliary floating H-Bridges (NPC-HBs) has been presented.

II. HYBRID TOPOLOGY

A. Neutral Point Clamped Converter

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [15]. These converters use clamped diodes and dc capacitors in order to generate ac voltage. Since all semiconductors are operated at a commutation voltage of half the dc-link voltage, the topology offered a simple solution to extend voltage and power ranges of the existing two level technology, which were severely limited by the blocking voltages of power semiconductors with active turn-on and turn-off capabilities. NPC converters can be extended to generate more output-voltage levels. The three level NPC features two additional diodes per phase leg as compared to a two level voltage source converter with a direct series connection of two devices per switch position. These so-called NPC diodes link the midpoint of the "indirect series connection" of the main switches to the neutral point of the converter. This allows the connection of the phase output to the converter neutral point N and enables the three-level characteristic of the topology.

In a 3-level NPC the DC bus voltage is split in two equal steps by capacitor banks. In this way, no extra DC sources are needed with respect to the standard 2-level inverter. The voltage between two switches is clamped through the diodes in the middle of the structure, called clamping diodes. Usually one diode with higher blocking capability or three diodes series can be connected. It is preferred to use series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor.

For a generic n-level NPC the diode reverse voltage is given by (1):

$$V_r = \frac{V_{dc}}{n-1} \qquad (1)$$

In 3-level NPC it is $V_{dc}/2$. Furthermore, this voltage drop is also the reverse voltage each switch has to block. Now it is clear that increasing the levels means a reduction of the stress over the components, considering the same DC bus voltage. Unfortunately, higher is the number of levels higher is the number of components. Increasing of one level involve the use of one capacitor, two switches and a lot of diodes more. In fact the number of clamping diodes used in a diode-clamped is related to the number of level by the following expression:

$$N_{Diodes} = (n-1)\,(n-2) \qquad (2)$$

B. Flying Capacitor Converter

Maynard and Foch introduced a flying-capacitor-based inverter in 1992 [28]. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform.

The three level Flying capacitor inverter is similar with diode-clamped topology. As for the diodes in diode-clamped, the capacitors series are drown to highlight the voltage drop they have to tolerate. Indeed, the voltage over the capacitors nearer to the switches is lower than the voltage over the ones nearer to the source in steady-state. The voltage over each capacitor is given as (3).

$$V_C = \frac{E}{n-1} \qquad (3)$$

Furthermore, these capacitors have the same function of the clamping diodes in diode-clamped converter: they keep constant the voltage drop between the buses to which they are connected. For this reason, they are called clamping capacitors. The voltage given in (3) is also the reverse voltage drop each switch must bear when all capacitors are fully charged.

In order to produce three levels, the switches are controlled so that only two of the four switches in each phase leg are turned ON at any time. In this representation, the labels S_{a1} and S_{a2} are used to identify the switches as well as the switching logic (1 = ON and 0 = OFF). Since the IGBT's are always switched in pairs, the complement transistors are labeled $\bar{S}_{a1}$ and $\bar{S}_{a2}$ accordingly.

One advantage of the flying-capacitor-based inverter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage.

Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are ON (conducting) be in a consecutive series. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels.

In addition to the (m-1) dc link capacitors, the m-level flying-capacitor multilevel inverter will require (m-1)× (m-2)/2 auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches.

C. Cascaded H-Bridge Inverter

The CHB multilevel inverter appeared first in 1988[16]. This converter topology has several advantages that have made it attractive to medium and high power drive applications. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link

supply for each H-bridge converter element must be provided separately. The ability to synthesize higher number of output voltage levels with an excellent harmonic spectrum utilizing low-cost low-voltage power semiconductors and capacitors.

The 3-level CHB is composed by the series connection of H-bridge power cells. For this reason, the CHB is also known as a multicell inverter. Each cell includes a single-phase 3 Level H-bridge inverter, a capacitive dc-link, a rectifier, and an independent or isolated voltage source provided by transformer secondaries or batteries. Usually, the rectifier consists of a three-phase-diode full-bridge rectifier. The dc voltage feeds a single-phase IGBT bridge, which generates the PWM output of the power cell. In this kind of multilevel converter, all the possible cell output levels are exploited. Some switches configurations are harmful for the converter and they must be avoided; for instance, the switches S_{k1} and $\bar{S}_{k1}$ are not allowed to be turned ON at the same time because this situation causes a shortcut of the source.

Note that there will be more than one switching state for some voltage levels (this is called inverter-output level redundancy), and this redundancy increases proportionally with the number of levels. These extra degrees of freedom can be used for control purposes. Moreover, considering the same DC source voltage, the output level amplitude and the switches reverse voltage drop given by (4) are greater here than in the diode-clamped or flying-capacitor.

$$V_r = V_{dc} \quad (4)$$

In order to increase the number of levels more cells have to be cascaded. High and low couple of switches can be defined in the respect of voltage output direction. The switching state of one cell S_k is determined by the logical value of two signals (S_{k1}, S_{k2}), which can be "1" and "0" representing the "ON" and "OFF" state of each switch, respectively. This leads to four different binary combinations that generate three different output voltages $+V_{dc}$, zero, and $-V_{dc}$.

A direct comparison between this cascaded converter and other multilevel topologies presented till here cannot be done because of different level amplitude. Imagining a substitution of the converter in an existing system, the better comparison hypothesis is to adapt the DC bus for the new converter keeping the same voltage value and splitting it. In this way, the voltage step amplitude for a n-level diode-clamped or flying-capacitor is given by (4) where V_{dc} is the total bus DC voltage. Whereas the voltage step amplitude of a cascade converter is given by (5).

$$\frac{2V_{dc}}{n-1} \quad (5)$$

The cascade H-bridge was the founder of cascade converter family and the simplest one. Each type of single-phase multilevel converter can be cascaded to obtain a leg. In this way, the levels each cell adds increase and is a good compromise between the required insulated sources and the number of output levels.

Cascade H-bridge converter is a very modular solution based on a wide commercialized product. This has a good repercussion on the reliability and the maintenance of the system since the cells have high availability, intrinsic reliability and a relatively low cost.

The main disadvantage of this converter consists in requiring several insulated sources that are not available in all applications. For instance, there are high costs in making insulated sources for induction motor drive systems because it requires isolation transformers. At the same time, this disadvantage makes cascade converters more suitable for photovoltaic or battery fed applications than the other types. Indeed, photovoltaic panels can easily be rearranged in several insulated sources to feed cascade H-bridge cells. A similar operation can even be done with battery banks.

Moreover, the insulated sources can be substituted with capacitors when the converter is used as active filter. In such kind of applications, the active power through the converter is theoretically zero, so there is no need to have power sources. Anyway, the converter has its own losses and the capacitors have to supply a little active power that discharges them. A simple control, sensing the voltage of each capacitor and exploiting either the intra-phase or joint-phase redundancies, can be done to avoid this problem. In this way, the active power to feed the converter is absorbed from the net and the capacitors feed reactive power only.

Comparison between Multilevel Converter Topologies:

While there are no limitations on the level of diode-clamped or flying-capacitor, which can be even or odd, cascade H-bridge can have only odd numbers of levels; indeed the first cell gives three levels whereas the others always add two levels more.

Totally, considering the cost of semiconductors and passive components, converter losses and simplicity of modulation schemes, cascaded H-bridge and diode-clamped inverters are more used in large motor drive applications. Flying capacitor inverters can be used in DC/DC converters since their phase voltage looks like that of a full-bridge phase shift modulated DC/DC converter.

D. Hybrid Multilevel Converter Topologies

Besides the three basic multilevel inverter topologies previously discussed, new MLI topologies based on the existing multilevel topologies have been proposed and classified as hybrid topologies.

Each power module of a hybrid MLI can be operated at distinctive DC voltage and switching frequency improving the efficiency and THD compensation characteristics of inverter. Nevertheless, conventional PWM strategies, which generates switching frequency at fundamental frequency are not appropriate for MLI's due to switching devices of the higher voltage modules, would have to operate at high frequencies only during some inverting instants. To achieve this control strategy, hybrid modulation methods have been proposed that provide to get higher power cells switched at low frequency and low power cells switched with high frequency.

Hybrid Multilevel Inverters promise significant improvements for medium voltage and high power industrial drives. Hybrid multilevel inverter minimizes the harmonic contents of output voltage without increasing the number of power devices. The use of various DC voltages in supply leads the Hybrid Multilevel inverter topologies in an effort to optimize the power processing of the entire system.

Hybrid topologies increase the

voltage and power rating of the converter, along with the number of levels, while enabling a reduction in the device switching frequency, like all other multilevel topologies with more levels. Hybrid multilevel inverters use different types of voltage sources in various parts of the inverter. These sources can be batteries, ultra capacitors, or fuel cell. By addition and subtraction of these voltages, more different output voltage levels can be generated with the same number of components, compared to a symmetric multilevel inverter. Higher output quality can be obtained with fewer cascaded cells and control complexity and output filters can be remarkably shrunk or even eliminated.

i) NPC-CHB Multilevel Converter

As the name suggests, it is a hybrid between the three level NPC and single-phase H-bridge cells connected in series at the output between the NPC and the load. The H-bridge dc side is a floating capacitor without a voltage supply. Hence, the addition of H-bridge stages only introduces more voltage levels but does not effectively increase the active power rating of the overall converter. The number of H-bridge cells connected in series usually varies between one and two.

The CHB stage acts as a series-connected active filter (AF).Although it contributes to enhance the power quality and reduce the common-mode voltages, it also introduces additional conduction and switching losses. The H-bridge dc-link capacitor voltage control, which is necessary to keep the desired voltage ratio between the NPC and the CHB, also adds to the complexity of the control system and requires additional voltage sensors.

Similar to the NPC-CHB, the traditional CHB has been modified by using a single dc-supply per phase, leaving the other cells floating. This simplifies the CHB topology by eliminating the complex phase-shifting transformer but limits the total active power rate of the converter. As with the NPC-CHB, special control of the floating dc-link capacitors is necessary.

ii) FC-CHB Multilevel Converter

This is obtained by cascading a three-level flying capacitor inverter with a flying H-bridge power cell in each phase. This topology has redundant switching states for generating different pole voltages. By selecting appropriate switching states, the capacitor voltages can be balanced instantaneously (as compared to the fundamental) in any direction of the current, irrespective of the load power factor.

The three-level Flying capacitor inverter with dc bus voltage of V_{dc} and FC voltage equal to $V_{dc}/2$, which can generate voltages of 0, $V_{dc}/2$, and V_{dc} with respect to point 0. A capacitor-fed H-bridge is cascaded to each phase of the inverter. The voltage across the H-bridge capacitor has to be maintained by external control. This combination can produce more voltage levels compared to the traditional flying capacitor converter

III. BLOCK DIAGRAM OF PROPOSED MULTILEVEL CONVERTER

The block diagram is shown in Fig 1. The hybrid topology is composed by a traditional three-phase three-level NPC inverter and also using flying capacitor inverter, connected with a single phase cascaded HB inverter in series with each output phase.

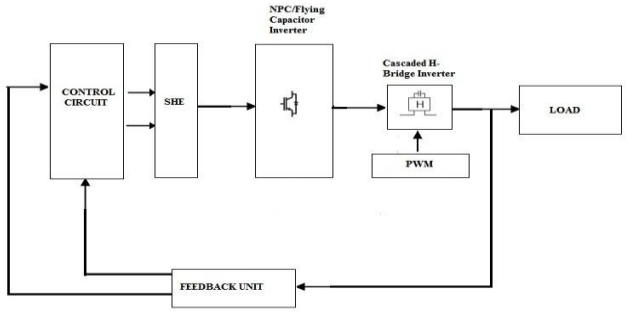

Figure 1 Block diagram of the proposed topology

For the modulation of the NPC inverter, the Selective Harmonic Elimination (SHE) method has been selected which has the advantage of very low switching frequency and hence low switching losses, while eliminating the lower order harmonics. With the use of SHE modulation, the fundamental output voltage of the converter is synthesized by the NPC converter and thus the series HB's will only need to supply reactive power, allowing for operation with floating capacitor DC-links. The HB should be modulated to compensate for the distortion created by the modulation of the NPC. This is done at a higher frequency using PWM technique.

A. Implementation of Flying Capacitor-CHB Hybrid Topology

The power circuit is illustrated in Fig 2, with only the H-bridge of phase a shown in detail.

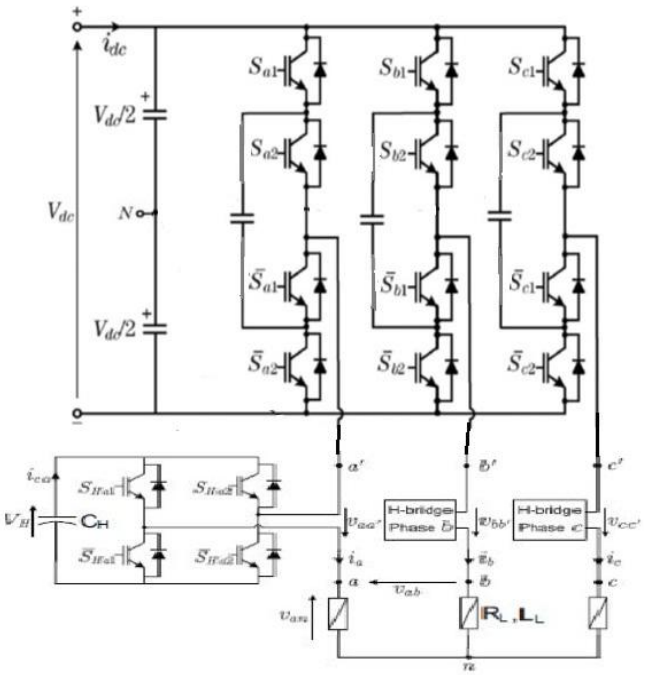

Fig 2.Proposed Flying Capacitor-CHB Hybrid topology power circuit

The H-bridge DC-links are not connected to an external DC power supply, and they consist only of floating capacitors kept at a constant voltage by the control strategy. The capacitor connected across the switches charges when S_{a1} is ON and S_{a2} remains OFF. At this condition the output voltage is $V_{dc}/2$. Then the capacitor starts

discharging when S_{a1} turned OFF with the output voltage of $-V_{dc}/2$.

B. *Switching states and voltage levels*

Table 1 summarizes the different switching states, the NPC and H-bridge individual output voltages and the total hybrid converter output voltage that can be generated for $V_H = V_{dc}/6$.

TABLE 1: SWITCHING STATES AND OUTPUT VOLTAGE LEVEL FOR V_{AN}

S_{a1}	S_{a2}	S_{Ha1}	S_{Ha2}	$v_{a'N}$	$v_{aa'}$	v_{aN}
1	1	1	0	$V_{dc}/2$	V_H	$4V_{dc}/6$
1	1	0	0	$V_{dc}/2$	0	$3V_{dc}/6$
1	1	0	1	$V_{dc}/2$	$-V_H$	$2V_{dc}/6$
0	1	1	0	0	V_H	$V_{dc}/6$
0	1	1	1	0	0	0
0	1	0	1	0	$-V_H$	$-V_{dc}/6$
0	0	1	0	$-V_{dc}/2$	V_H	$-2V_{dc}/6$
0	0	0	0	$-V_{dc}/2$	0	$-3V_{dc}/6$
0	0	0	1	$-V_{dc}/2$	$-V_H$	$-4V_{dc}/6$

Switching States of the NPC-CHB or Flying Capacitor-CHB Hybrid topology depends upon floating dc-link capacitor. Some redundancies for the zero output voltage of the H-bridge were omitted in the table. At $V_H = V_{dc}/6$ there are 9 different output voltage levels, instead of the original 3 provided by the NPC inverter.

IV. CONTROL STRATEGY

Each series H-bridge converter is independently controlled by two complementary references, as shown in Fig.3. The first reference $v^*_{aa'}(f_n)$ corresponds to the inverse of the harmonics remaining from the SHE pulse pattern, calculated as described in the previous section from the difference between the NPC pulsed voltage pattern and its sinusoidal voltage reference.

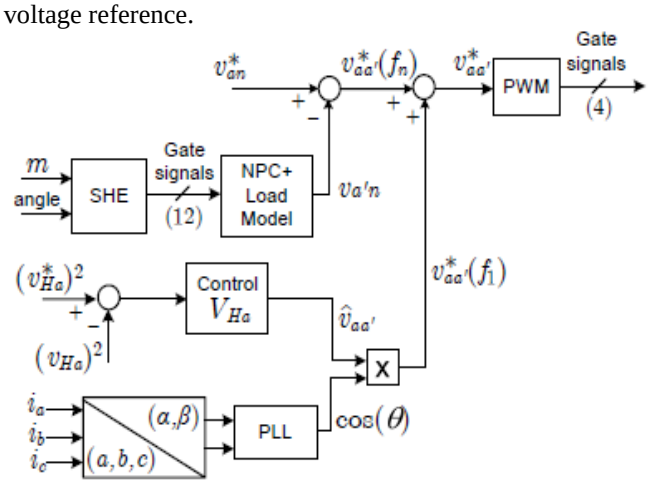

Fig. 3 H-bridge control diagram for phase *a*

This calculation provides a fast and straightforward distortion estimation allowing for simple feed-forward compensation. Moreover, this voltage does not have a fundamental voltage component and hence it does not affect the floating average DC-link capacitor voltage. Nevertheless, to achieve start-up capacitor charge and to compensate voltage drift due to transient operation, an additional reference component for DC link voltage control is included. This second component of the voltage reference $v^*_{aa'}(f_1)$ corresponds to a signal in phase with the load current. This voltage is used to inject small amounts of active power into the cell in order to control the H-bridge DC-link voltage at its reference value v^*_H.

During operation, the fundamental load current is generated by the NPC converter. In order to synchronize the voltage reference $v^*_{aa'}(f_1)$ with this current, a phase lock loop (PLL) algorithm is used, which guarantees zero phase shift between both signals and therefore maximizes the active power transfer to the capacitors for any power factor. The magnitude of this voltage reference is obtained from the DC-link voltage controller shown in Fig. 3. For the design of this voltage controller, the dynamic model (7) of the dc-link voltage v^*_{Ha} as a function of $v^*_{aa'}$ is used. This model has been developed based on an instantaneous active power balance applied to the simplified cell circuit of Fig. 4.

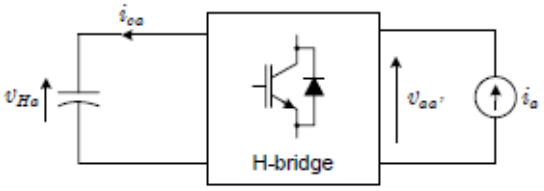

Fig.4. Simplified H-bridge circuit for dynamic modeling of dc-link voltage

In this circuit the fundamental phase current imposed by the NPC converter and the load is modelled as a sinusoidal current source of value $i_a(t) = \hat{i}_a\cos(\omega t)$. If a fundamental voltage $v^*_{aa'}(t) = \hat{v}_{aa'}\cos(\omega t)$ is applied to the cell terminals, the input power is expressed as (6)

$$p_i(t) = i_a(t).v_{aa'}(t) = \frac{\hat{i}_a.\hat{v}_{aa'}}{2}\left[1+\cos(2\omega t)\right] \quad (6)$$

This input power can only be stored in the dc-link capacitor producing a variation of the dc-link voltage as shown in (2)

$$\frac{C_H}{2}.\frac{dv^2_{Ha}}{dt} = \frac{\hat{i}_a.\hat{v}_{aa'}}{2} + \left[1+\cos(2\omega t)\right] \quad (7)$$

If the component at 2ω that only causes pulsation in the dc-link voltage is discarded, the relation between the square value of the dc-link voltage and the fundamental output cell voltage can be expressed as (8)

$$\frac{C_H}{2}.\frac{dv^2_{Ha}}{dt} \approx \frac{\hat{i}_a.\hat{v}_{aa'}}{2} \quad (8)$$

An undesirable characteristic of (8) is its nonlinearity with respect to v_{Ha}. This can be dealt with by linearization or by simply introducing the auxiliary variable $x = v^2_{Ha}$ and controlling x directly. Finally, the transfer function can be expressed as (9)

$$\frac{X(s)}{\hat{v}_{aa'}(s)} \approx \frac{\hat{i}_a}{C_H.s} \quad (9)$$

The first order and can be easily controlled by a PI regulator to follow the constant reference v^2_{Ha}.

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Nevertheless, its variable gain given by $\hat{i}_a$ would result in different dynamic performance at different operating conditions. To account for this effect, the voltage PI controller is modified to include a variable gain inverse to the load current reference magnitude $|\hat{i}_a^*|$.

V. MODELING OF HYBRID TOPOLOGY

The modeling is carried out using MATLAB/SIMULINK to evaluate the proposed hybrid topology and its control method.

Typical Parameters involved in modeling of hybrid converter are tabulated in Table 2

TABLE 2 PARAMETERS INVOLVED IN MODELLING OF HYBRID CONVERTER

S.No	Parameter	Value
1.	Input Voltage V_{dc} (Volts)	180
2.	Number of bridge arms	3
3.	Snubber resistance R_s (Ω)	$1e^5$
4.	Snubber capacitance C_s (F)	Inf
5.	Power Electronic device	IGBT/Diodes
6.	Diode Forward Voltage V_f (Volts)	0.8
7.	DC Capacitors C_1,C_2 (μF)	20
8.	Load Resistance R_L (Ω)	10
9.	Load Inductance L_L (mH)	3

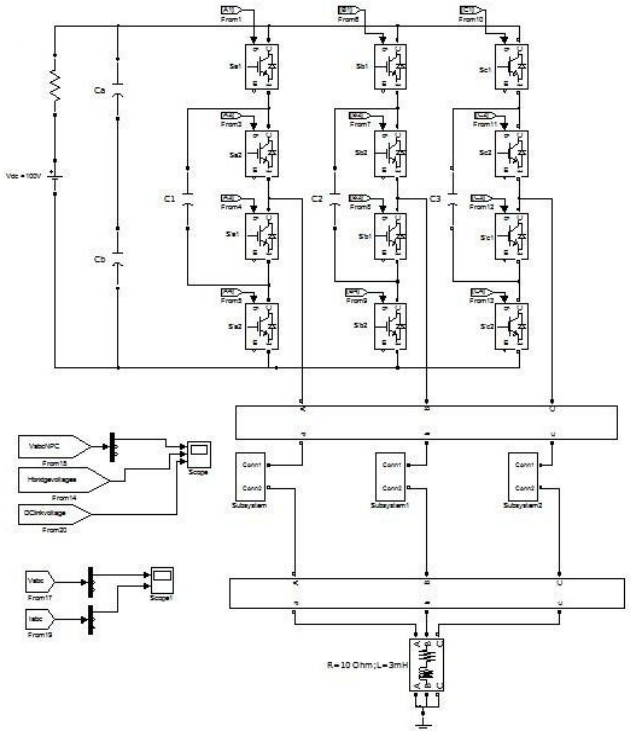

Fig.5. Simulation Model of FC-HB Hybrid Converter

Fig. 5. Shows the Simulink model of the NPC-HB Hybrid Converter feeding a linear load with values R_L = 10 Ω and L_L = 3 mH. Here, the converter is operated with V_{dc} = 180 V while the HB dc-link voltage reference was set to 30V.

VI. RESULTS

The results of the NPC inverter operating without HB compensation is shown in Fig.6. Here, the NPC inverter is modulated by a five-angle SHE pattern and m = 0.8. The first waveform corresponds to the NPC inverter output phase voltage $v_{a'N}$ which results in the nine-level load voltage waveform v_{aN} as seen in second waveform. Finally, third waveform shows the resulting output current waveform with its characteristic low-frequency distortion.

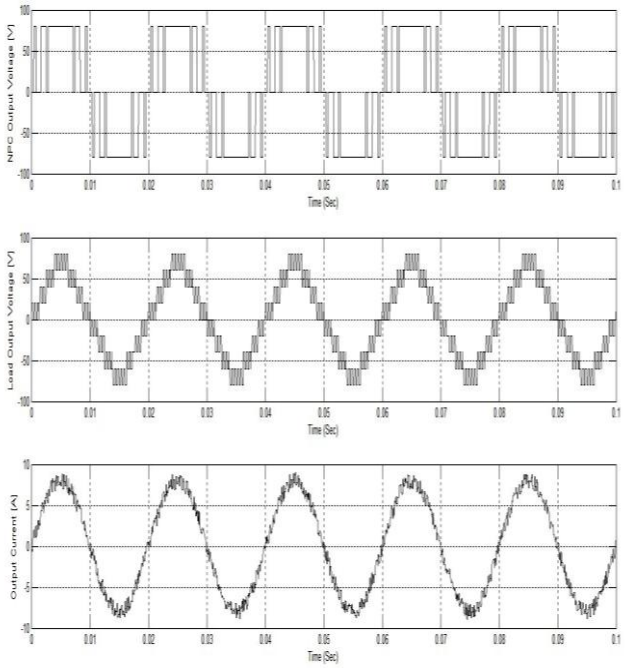

Fig. 6. Simulated Output for NPC Converter Operation at 50Hz with *m*=0.8

In comparison to the above results, the full hybrid topology results are shown in Fig.7. First waveform shows the three-level NPC output voltage v_{aN} generated under the same conditions while second waveform shows the output voltage of the respective HB $v_{aa'}$. Note that the higher switching frequency compared with the NPC output. An additional distortion can be appreciated due to the semiconductor drop, which will not be relevant for higher voltage applications. The HB dc-link voltage is shown in third waveform which is controlled to be the desired voltage of V_H= 0.167V_{dc}. Moreover, it can be noted that, in fifth waveform, different voltage levels are applied to the load voltage, causing less distortion in the output inverter waveforms than in the waveforms of Fig.6. The sixth waveform is the current waveform which is seen clearly with a highly sinusoidal shape compared with the output current waveform without the HB harmonic compensation in Fig. 6. Hence, it is clear that the current waveform improvement has been achieved with the hybrid inverter.

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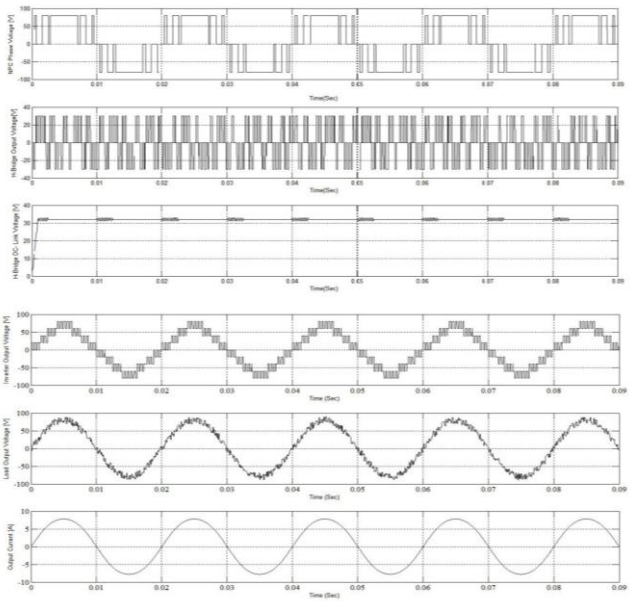


Fig. 7. Simulated Results of an NPC-HB Hybrid Converter at 50Hz with m=0.8

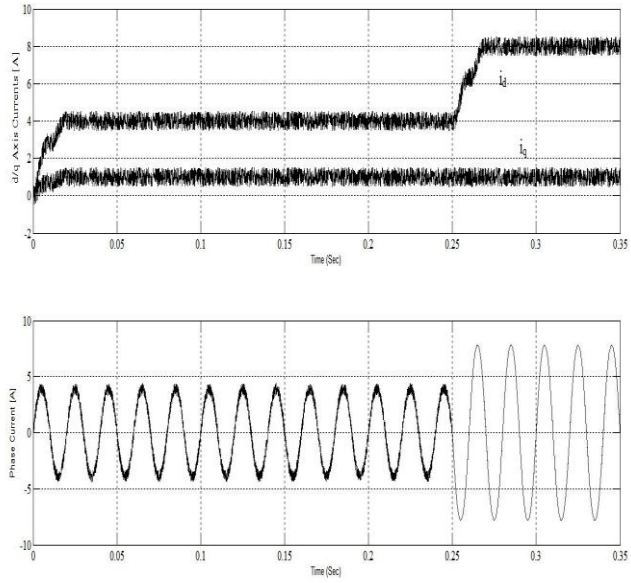


Fig.8.Simulation results NPC-HB for Closed Loop Current Response (a) Measured currents in the synchronous frame d/q. (b) Phase current

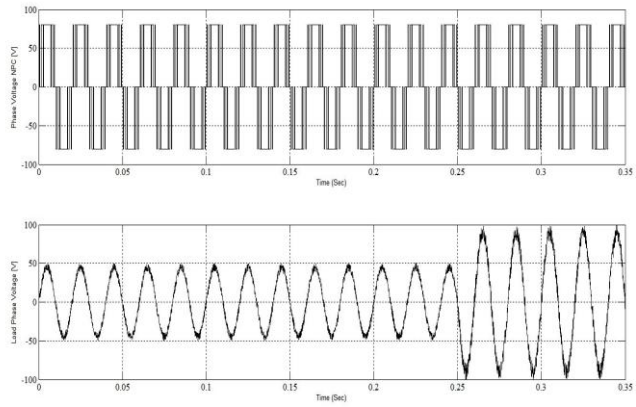


Fig.9. Voltage during current step. (a) NPC voltage response. (b) Total load phase voltage.

The current loop dynamic response is shown in Fig.8 and Fig.9, where a step from 4 to 8 A in the d-axis current is commanded while the q-axis current reference is kept constant. No significant oscillations are present in the NPC voltage as shown in First waveform, which keeps operating with the five-angle pattern, even during the current transient. During the transient, however, small oscillations are present in the currents due to the limited compensation capability of the HBs, which is a result of their low voltage, and due to the limited amount of energy stored on them. Nevertheless, this additional oscillation decreases rapidly once the NPC stabilizes and reaches a quasi-steady state.

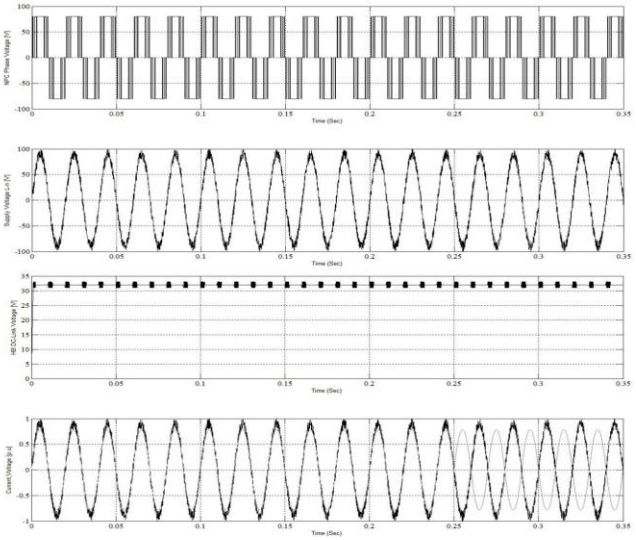


Fig.10. Simulated Results of NPC-HB in Regenerating mode

Fig.10. presents the simulation results for the hybrid topology and control method when it is used as an active rectifier Note that at t = 0.25s, a change from the feed mode to the regenerative load mode has been demanded. This results in the change in the polarity of the input current i_a and in the NPC SHE voltage output v_{aN}. The phase to neutral supply voltage van clearly shows the multilevel stepped waveform introduced by the NPC rectifier and the HB series filter, which results in a high quality input current. Though there is a change in the direction of power flow, the proposed dc-link control method exhibits good performance which can be observed in the HB dc-link voltage V_{Ha}.

The simulated results of FC converter and FC-HB Hybrid Converter are shown in Fig.11 and Fig.12. It is observed that the current waveform improvement has been achieved with the hybrid inverter.

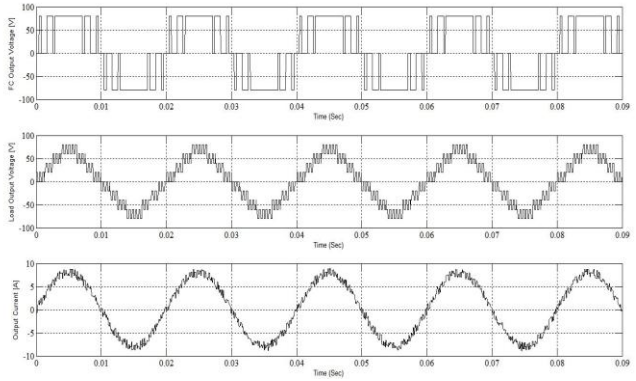


Fig 11.Simulated results of FC Converter Operation at 50Hz with m=0.8

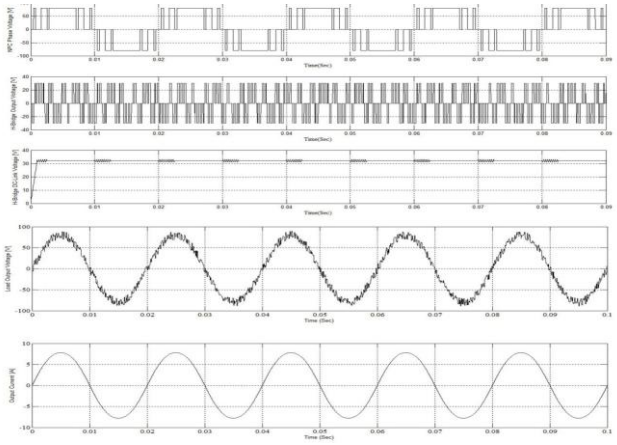
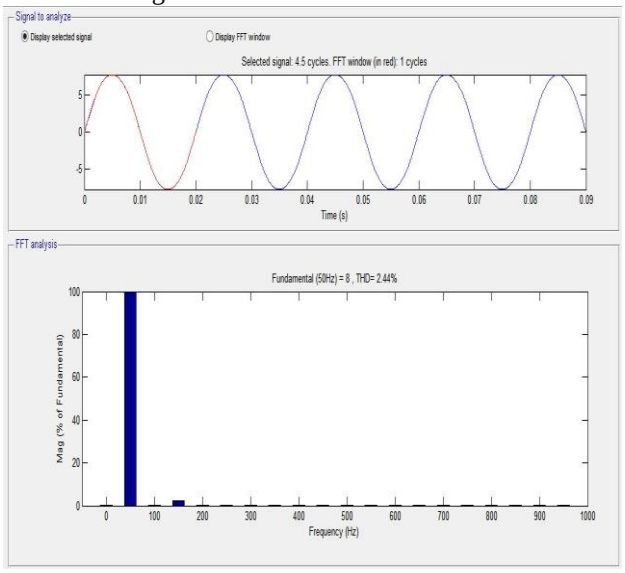
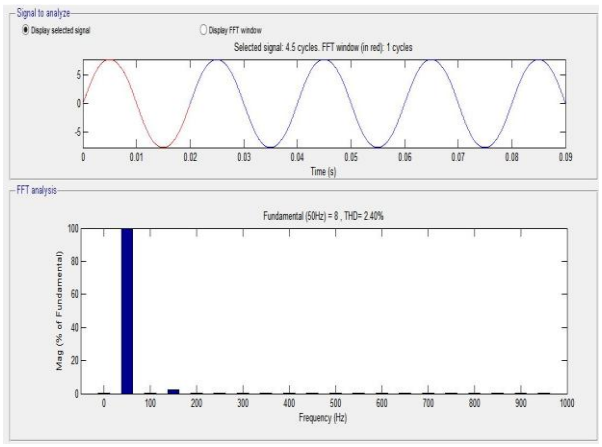


Fig.12.Simulated Results of FC-HB Hybrid Converter at 50 Hz with m = 0.8.

The total harmonic distortion is calculated by the FFT analysis of the converter. Total harmonic distortion is a measurement of the sum value of the waveform that is distorted. The FFT analysis is carried out for the corresponding Current waveforms of the NPC Converter, NPC Converter with H bridge, Flying Capacitor and Flying Capacitor with H-Bridge and are tabulated in Table 3. It is clear that there is a reduction of THD in hybrid topologies. FFT analysis of NPC-HB Converter and FC-HB Converter are shown in Fig. 13.



(a)NPC-HB Converter



(b) FC-HB Converter

Fig.13. FFT Analysis of current waveform

TABLE 3 COMPARISON OF THD IN DIFFERENT TOPOLOGIES

Topology	THD (%)
NPC Converter	9.32
FC Converter	9.28
NPC-HB Converter	2.44
FC-HB Converter	2.40

VII. CONCLUSION

In this paper the hybrid topologies of multilevel converters have been proposed and implemented for NPC, NPC-HB, FC and FC-HB converters. The series connection of a SHE modulated NPC and an HB multilevel inverter with a control scheme is presented to control the floating voltage source of the HB stage. The addition of the HB series active filter or additional converter stage is not intended to increase the power rating of the overall converter. The power quality of the NPC Bridge which has a relatively low switching frequency is improved. Since no changes are made to the power circuit and modulation strategy of the NPC inverter, the series HB power circuit and its control scheme can be easily added as an upgrade to the existing NPC-driven applications. The simulation results show an improvement in the current waveforms and good agreement with the proposed topologies.

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