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Design and Implementation of Phase Modulation using PLL for Polar Transmitter

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Abstract: ***In this paper the phase modulation of polar transmitter has been implemented. The circuit for implementing phase modulation consists of Phase Lock Loop (PLL), Sigma Delta Modulator (SDM) and differentiator. The input signal is applied at the differentiator which will convert phase component to the frequency of the signal. The obtained frequency signal is given to the SDM which will convert the analog signal to the digital signals. The SDM should have four bits of resolution, equivalently 36 dB signal-to-noise-and-distortion-ratio (SNDR) for a 200 kHz bandwidth. For supply voltages from 2.5 V to 3 V, the current supply is desired to be less than 20 mA. The PLL consists of the reference signal of 125MHz, and output voltage around 2-3GHz with the VCO gain of 0.277GHz/V. The circuit of PLL, SDM and differentiator are implemented on the Cadence Virtuoso platform.***

Index Terms: ***Polar transmitter, phase modulation, Phase lock loop, Sigma delta modulator, differentiator.***

I. INTRODUCTION

The polar modulation techniques use magnitude and phase [1]. This ensures the application of the two resulting modulating components (phase and magnitude) differently and more efficiently. The phase component PM is applied using the PLL while the amplitude component AM is applied at the PA. Since the amplitude of the phase-modulated signal produced by PLL remains constant, it can be amplified using very efficient, saturated or compressed amplifiers. This dramatically reduces dc power consumption by the transmitter [1]. Mapping the complex signal trajectory to its phase and amplitude components is a nonlinear process which is complicated as the trajectory approaches the origin [1]. The separate phase and amplitude signals actually accelerate near the origin. Furthermore, it is not uncommon for the phase and amplitude signals to abruptly change directions [1]. These effects widen the spectrum of the modulation signals.

The Polar transmitter is shown in Fig 1. A numeric algorithm (Coordinate Rotation Digital Computer-CORDIC) transforms the I/Q signal components to polar coordinates r/θ. The phase (θ) of the signal is modulated in a PLL onto a constant-envelope waveform centered at the carrier frequency. This constant envelope signal is then amplified in an efficient saturated power amplifier [4].

The waveform envelope is reconstructed by modulating the PA gain or supply voltage. At the core of the polar transmitter lies the process of phase modulation and amplitude modulation and signal reconstruction.

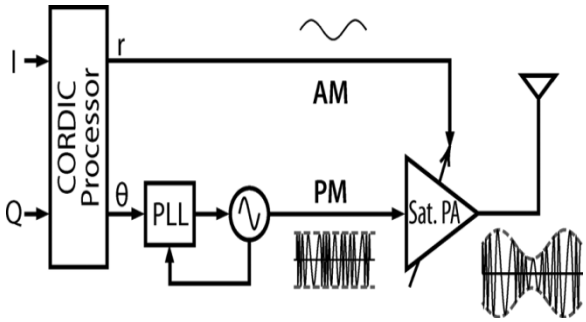

Fig 1 - Conventional Polar transmitters [5]

The phase modulation for polar transmitter is done using PLL, SDM and a differentiator. PLL consists of PFD, loop filter, charge pump, VCO and MMD. The SDM consists of op-amp, comparator and DFF. The SDM is one bit output. Since we need four bit output, the SDM is connected to the Decimation filter so that it will convert the one bit output to four bit output. The op-amp is designed using gm-cell.

II. PROJECT

The Core technology of transmitter uses a highly efficient switching-mode power amplifier and PLL. This project gives an idea about only how the phase modulation is done in the polar transmitter. The polar transmitter uses a phase-locked loop to apply phase modulation directly to the synthesized RF carrier and effectively eliminates I/Q converter with its spurious problems. A conventional polar transmitter is as shown in the Fig 1 [5]

A simplified block diagram of a phase modulation of polar transmitter is shown in Fig. 2. It consists of a PLL, SDM and a differentiator at the input. The PLL block consists of PFD, charge pump, loop filter, VCO and MMD. The feedback minimizes the phase error between the reference signal (REF) and output of the VCO. It produces an output signal at a frequency given by $N * Fref$, where N is the effective divide ratio of the MMD and Fref is the reference frequency. The divide ratio is always an integer. The SDM allows for a non-integer average value by alternating between two or more integers divide ratios while accentuating the spectrum of quantization noise to high frequencies, where it is attenuated by loop rolloff [6]. Since the loop bandwidth must be restricted to suppress out-of-band quantization noise, the DSM can be driven digitally to apply PM [7-10].

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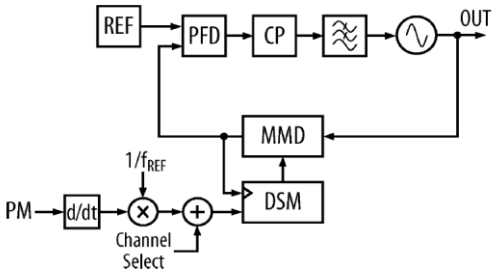

Fig 2-Phase lock loop with delta sigma modulator [5]

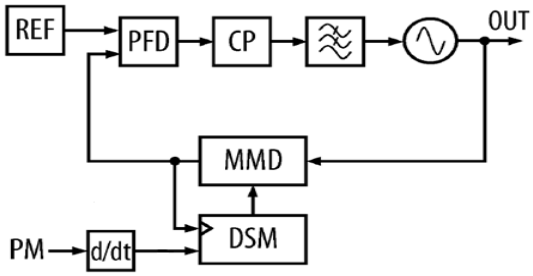

Fig 3- Circuit for the Phase modulation of Polar transmitter.

Fig 2 is for the multi mode transmitters. The circuit is modified for single mode transmitter. In Fig 3, the channel select is not taken into consideration as it will be complex to design.

III. CIRCUIT DESIGN FOR THE IMPLIMENTATION OF PHASE MODULATION OF POLAR TRANSMITTER

To implement phase modulation, the block diagram is divided into three parts, i.e., PLL along with VCO and MMD, SDM with Decimation filter and differentiator.

The PLL consists of reference signal, PFD, Charge pump, loop filter along with VCO and MMD. The reference signal is taken as 125Mhz as the specification of Polar transmitter.

A. PFD

The circuit diagram of proposed PFD is as shown in Fig 4. It works similar to conventional PFDs. These PFDs is basically constructed with two GDI (Gate Diffusion Input) cells. A basic GDI cell contains four terminals – G (common gate input of nMOS and PMOS transistors), P (the outer diffusion node of PMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors) [11]. This technique allows reducing power consumption, propagation delay, and area of digital circuits [12].

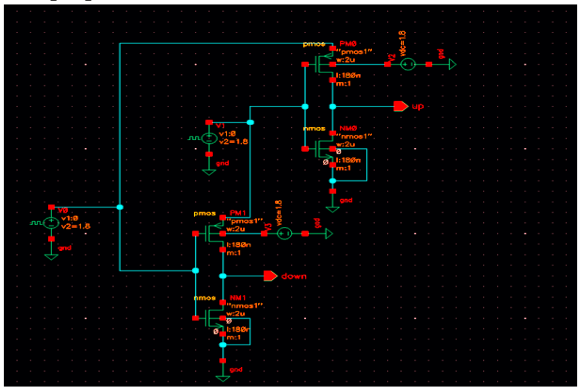

Fig 4- circuit of PFD using GDI cell.

B. CHARGE PUMP

Charge pump is used to convert the phase error signal which is obtained from the PFD to the error analog signal. The signal which is given to the charge pump will be digital as those are the outputs of the PFD. Since the PFD is the digital circuit. Charge pump will convert the digital error signal into the analog error signal and gives to the loop filter as shown in the Fig 5.

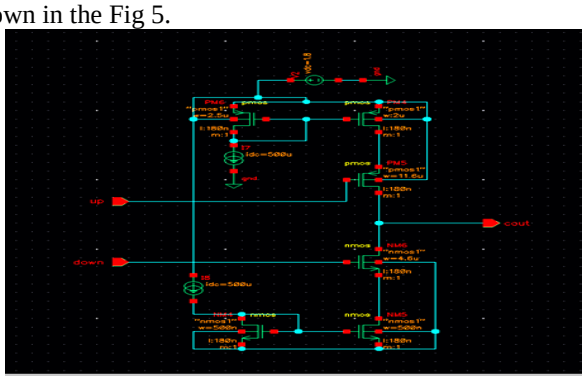

Fig 5 – Schematic representation of the charge pump.

C. LOOP FILTER

The function of a charge pump and loop filter is to take the digital UP and DOWN pulses from the PFD and convert them into an analog control voltage, Vctrl. The Fig 6 gives the combined circuit of the charge pump and the loop filter.

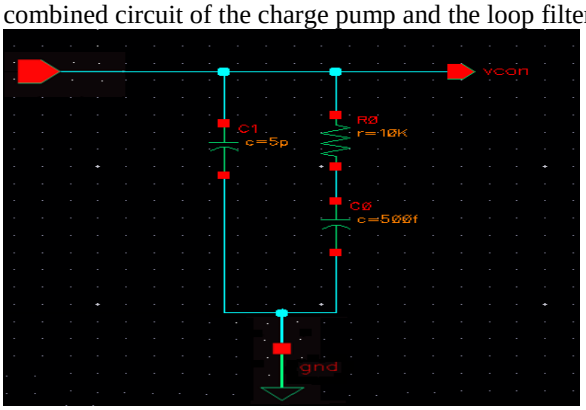

Fig 6 loop filter components.

D. VCO

In selecting of VCO, based on Ring oscillator and LC oscillator, current starved VCO is used which is a Ring oscillator. It is used because of its advantages like wide frequency range, easy to design, integrate and model, easy to generate multi-phase outputs, requires smaller area. Fig7 gives the ring oscillator which had been implemented.

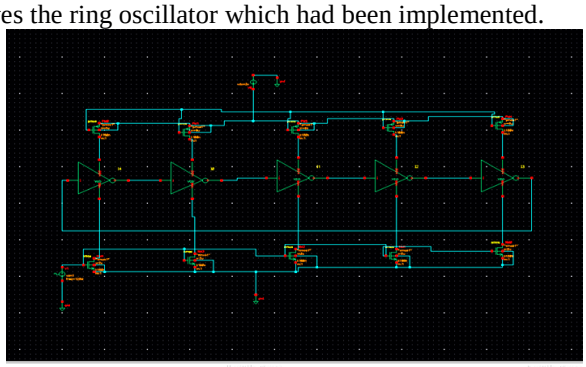

Fig 7 – schematic representation of VCO

E. MMD

The dual-modulus approach is used in many high speeds low-power designs [13-18]. A high speed programmable divider is used an extension of a dual-modulus divider in which the overall divide-by-2 sections are replaced by divide-by-2/3 blocks [19, 22]. Based on the dual-modulus topology, multi-modulus divider structure is as shown in Fig.8, which consists of a synchronous divide-by-4/5 counter as the first stage, an asynchronous divide-by-64 counter as the second stage, and several gates as the controlled stage. The control block eliminates MC controlling the divided ratio of 4 or 5 of the synchronous counter, which is a combination logic circuitry. Depending on the logic value at MC, the first stage division ratio is 4 (MC = 0) or 5 (MC = 1).

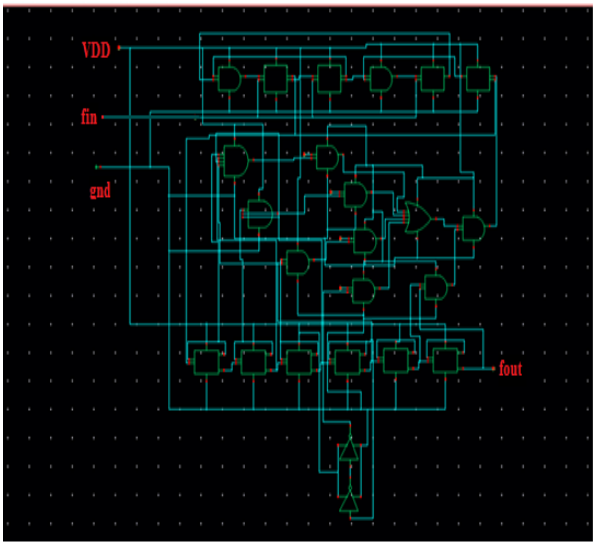

Fig 8 – Schematic representation of MMD.

IV. CIRCUIT DESIGN FOR THE IMPLEMENTATION OF SDM AND DECIMATION FILTER.

A. Gm- CELL

The main building block of SDM is an integrator. A Gm-cell and a capacitor can be used to realize an integrator in Gm-C technology as shown in Fig 9 [24-27].

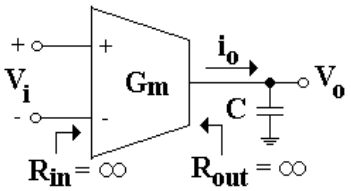

Fig 9 - Single-ended Gm- Cell [26].

The Fig 10 gives the schematic of the Op amp which have done using Gm Cell

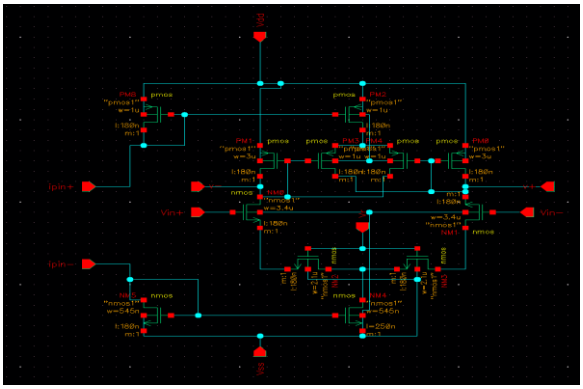

Fig 10 - circuit of the Op amp used in SDM.

B. COMPARATOR DESIGN

To combine the sample-and-hold function and the comparator function in a quantizer, the latched-type comparator is the best choice. Fig 11 depicts the Schematic representation of the CMOS latched-type Comparator in the quantizer design [28]

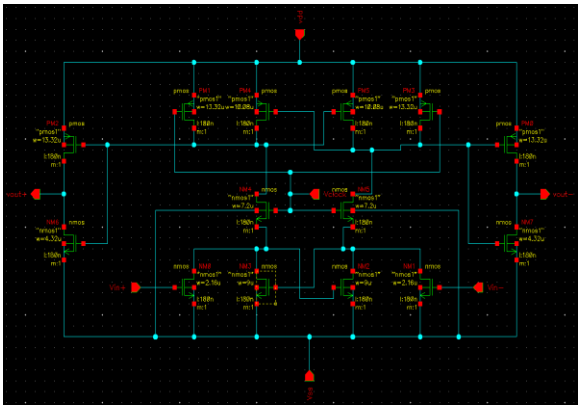

Fig 11- Schematic representation of the CMOS latched-type Comparator.

C. TSPC- DFF

In order to convert the return-to-zero (RZ) output of the comparator to a NRZ output, a D flip-flop is added after the latched-type comparator. It is too slow for usual static D flip-flop to use in a 560 MHz sampling system, therefore, a TSPC D flip-flop is chosen. Fig 12 shows the schematic representation of the design of the TSPC D flip-flop [23].

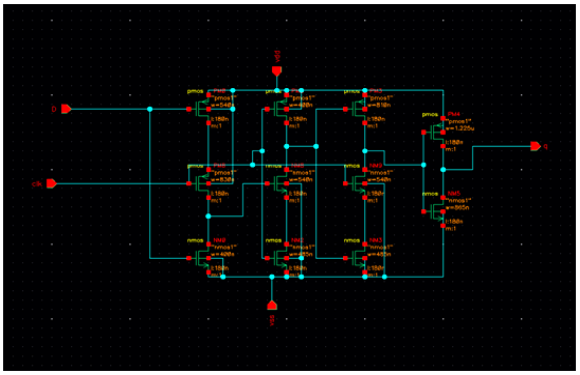

Fig 12 - Schematic representation of the TSPC D flip-flop.

This D Flip-flop design also used in designing of Decimation Filter where Vout is used as output, but, in Quantizer Design, in order to convert the return-to-zero (RZ) output of the comparator to the NRZ output we consider Vout' as output.

D. DAC

A feedback DAC is required for Gm-C implementation of the SDM. The DAC should be linear and fast, therefore, 1-bit DAC is designed. The feedback DAC for the SDM using 180nm is implemented by a simple differential-pair to convert the output voltage to a current level. The adder is done by current addition of the Gm-cell current output and the current output of the DAC. The effective feedback voltage is determined by the feedback current level of the DAC. In this, 180nm design, an effective feedback voltage of 1V has been chosen and hence the DAC feedback current level was chosen to be 120 µA at 3V differential-pair input. Fig 13 shows the schematic of current steering feedback DAC.

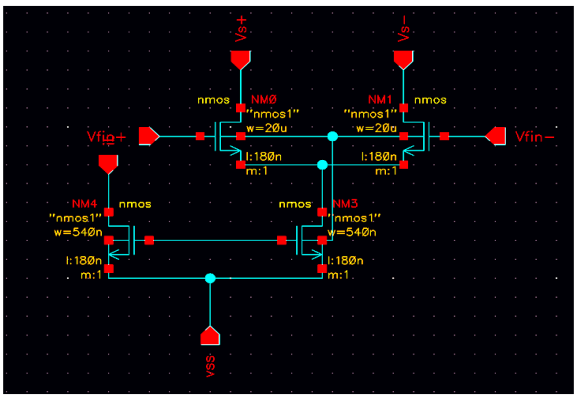

Fig 13 - circuit of the DAC.

E. DECIMATION FILTER

The Decimation filter for the SDM output is implemented as a Complex low pass filter (LPF), i.e., the input stream of band pass signal is modulated into two low pass streams and filtered separately. This low pass filter has as its first stage; a CIC filter followed by FIR filters for compensation and band limitation to eliminate aliasing caused by down sampling. The realization of the filter using full adder and the D flip-flop is presented in the following sections. In this, the full adder cell, CIC filter, FIR filter, and Ripple Carry Adder (RCA) designs are presented.

The Full Adder cell forms the most important part of the decimation filter as in the Fig 14. This implements the multiplication operation along with the shifting function, which can be hard-wired. Thus, the performance of the individual cells directly influences that of the entire system. This requires the full adder to operate at a high-speed, and consume low power.

The expressions for the sum and carry outputs for the full adder are given by,

$$S = A \oplus B \oplus C \quad (1)$$

$$C_{out} = AB + BC_{in} + C A \quad (2)$$

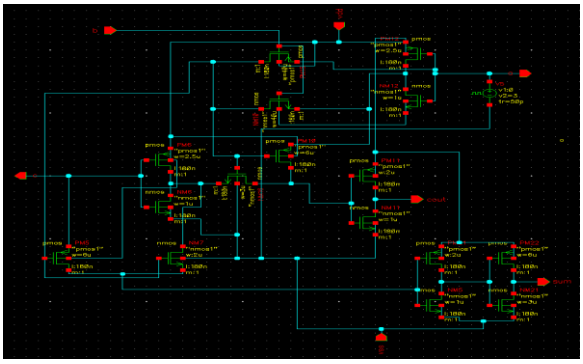

Fig 14 - Full Adder Cell implementation in Cadence

The CIC filter receives the samples from the modulator and operates at the highest sampling frequency of the filter. This filter needs to attenuate the quantization noise that aliases into the desired band of the modulator and hence it should be greater order than the modulator. The SDM whose output serves as the input to the filter is of third order [29]

The output from the SDM has a 1-bit word length and hence the output of the CIC filter should have a word length of 4-bits. The realization of the third order filter use a cascade of the computational element is shown in Fig 15 [30-31].

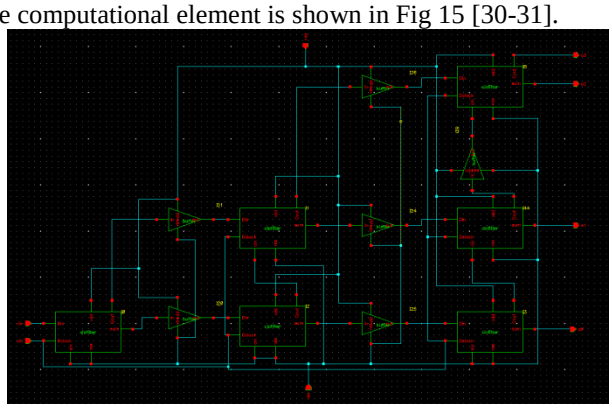

Fig 15 – Schematic representation of third Order CIC Filter

The Decimation Filter for the SDM output is implemented as a Complex low pass filter (LPF). This low pass filter comprises the first stage, a CIC filter followed by FIR Filters and RCA for compensation and band limitation to eliminate aliasing caused by down sampling. The Decimation filter is implemented by integrating the CIC Filter, FIR Filter and RCA. The Schematic design of the Decimation Filter is shown in Fig 16.

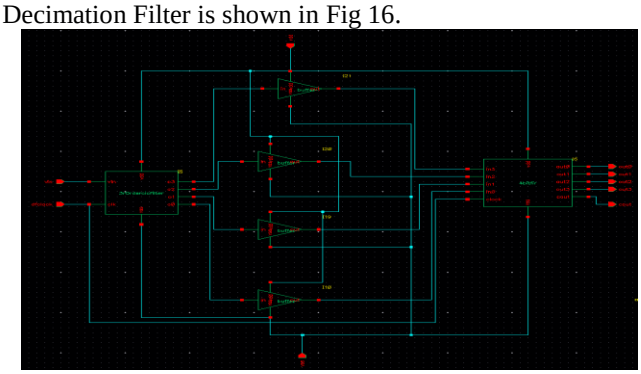

Fig 16 - The Schematic representation of the Decimation Filter

F. DIFFERENTIATOR.

A differentiator circuit consists of an operational amplifier, resistors are used at feedback side and capacitors are used at the input side as shown in Fig 17. The circuit is based on the capacitor's current to voltage relationship:

$$I = C\frac{dv}{dt} \quad (3)$$

Where, I is the current through the capacitor, C is the capacitance of the capacitor, and V is the voltage across the capacitor.

The current flowing through the capacitor is proportional to the derivative of the voltage across the capacitor. This current can be then, connected to a resistor, which has the current to voltage relationship:

$$I = \frac{V}{R} \quad (4)$$

Where, R is the resistance of the resistor.

Note that the op amp input has a very high input impedance (it also forms a virtual ground) so the entire input current has to flow through R.

If Vout is the voltage across the resistor and Vin is the voltage across the capacitor, we can rearrange these two equations to obtain the following equation:

$$Vout = -RC\frac{dVin}{dt} \quad (5)$$

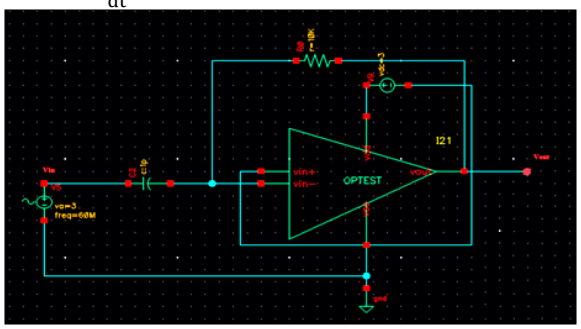

Fig 17 - Schematic representation of the differentiator.

V. RESULTS SIMULATION AND ANALYSIS

Table 1 - Specifications of the Polar transmitter

Parameters	Values
Reference frequency	125MHz
Output Frequency	2 to 3GHz
Lock range	1MHz
Dampling Factor (ζ)	0.7
Phase margin	50°
Vdd	3V

Fig 18 shows the complete circuit of the PLL, which contains the symbols of the PFD along with the CP and LP, VCO and MMD.

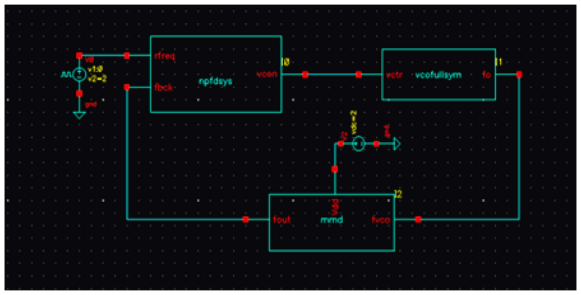

Fig.18 - complete PLL.

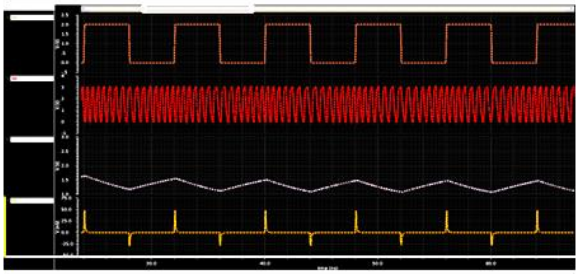

Fig 19 - gives the transient analysis of the complete PLL.

Fig 19 gives the transient analysis of the complete PLL for the time interval of 200ps. The inputs to the PFD system are reference signal, i.e., net6, and the output from the MMD i.e., net4. The output of the MMD (net4) acts as the input to the PFD system. The VCO output is varied from 2GHz to 3GHz.

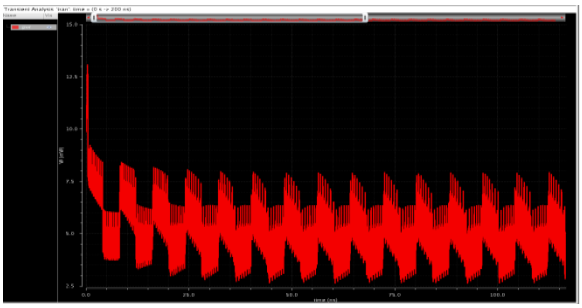

Fig 20 - Power measurement waveform of complete PLL

The Fig 20 shows power measurement waveform of complete PLL for a power supply 3V. By using calculator in cadence, the power consumed by complete PLL is 4.277E-3W (4.277mW).

Fig 21 shows the circuit of the SDM with decimation filter. Decimation filter will convert the one bit output to four bit output.

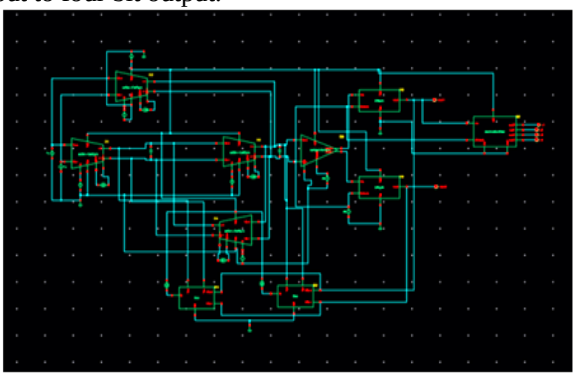

Fig 21 – Schematic representation of SDM with Filter

Fig 22. shows the transient analysis of the SDM with decimation filter for the time interval of 200ps. The signal net5 of 70GHz is applied to the SDM as input. The signal vout1 is SDM output. The outputs with filters are V1, V2, V3 and V4.

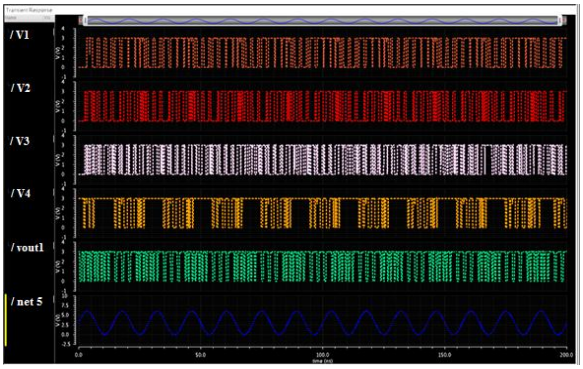

Fig - 22 Output of SDM with Decimation Filter

The Fig 23 shows power simulation result of SDM with Decimation filter. The corresponding power value of the result waveform is 57.9e-3 (57.9mW).

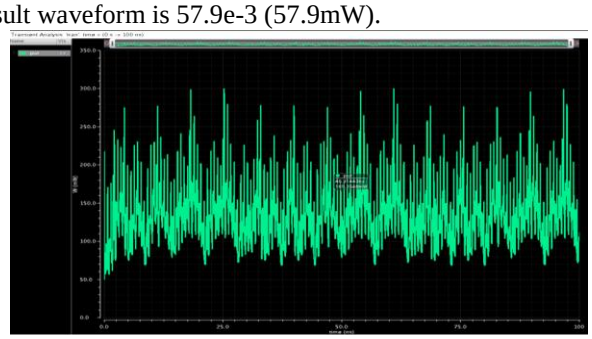

Fig 23 - Power simulation result of SDM with Decimation filter.

The Fig 24 shows spectrum result of SDM which gives the values of SNDR, SNR, and ENOB.

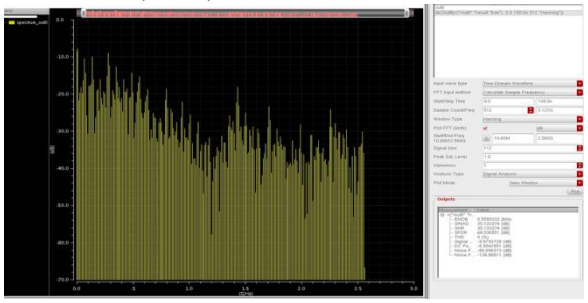

Fig 24 - Spectrum result of SDM with decimation filter.

Fig 24 shows the complete phase modulation circuit for polar transmitter. It contains combination of SDM, PLL with the differentiator as shown in the Fig 25.

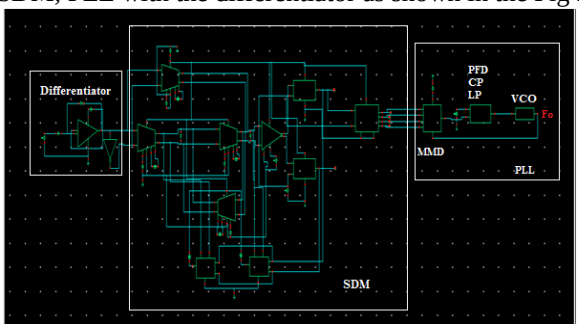

Fig 25 - Complete Phase modulation circuit for polar transmitters

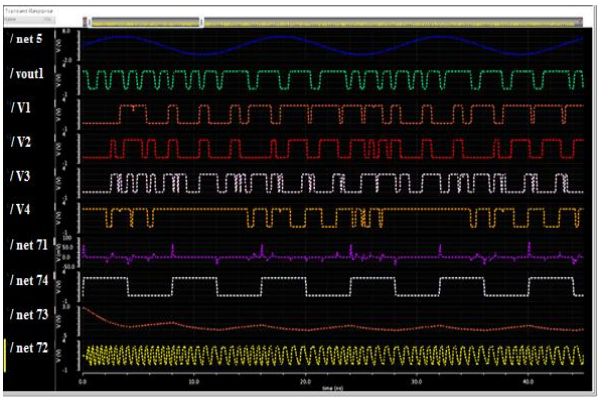

Fig - 26 Final Output Of combination of PLL and SDM for phase modulation.

Fig 26 gives the transient analysis of the phase modulation circuit for the time interval of 200ps. It consists of three blocks of differentiator, SDM and PLL. The input signal (net5) is given as the phase component to the differentiator. The differentiator converts phase component of the signal to the frequency signal. The obtained frequency signal will be given to the SDM and PLL. The control voltage signal is fed to the VCO to change the frequency. Finally the frequency modulation is obtained at the output of the PLL at the VCO. Net71 is the MMD output, net74 is the reference signal, net73 is the PFD system output i.e., the output of the loop filter and net72 is the final output which is obtained at the VCO. The obtained output at the VCO is frequency modulated wave. The summary of the results are tabulated in table 2 for the complete Phase modulation of the polar transmitter.

The Fig 27 shows power simulation result of phase modulation of polar transmitter. The corresponding power value of the result waveform is 99.4E-3 (99.4mW).

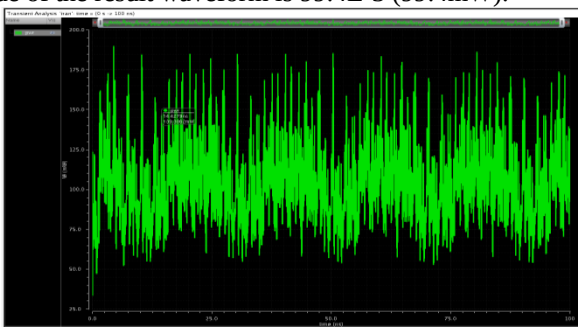

Fig 27 - Power waveform of Phase modulation of polar transmitter.

Table 2 - Summary of the final output of the Polar modulation of phase modulation

Parameters	Values
Technology	180nm
Reference frequency	125 MHz
Input frequency	70 MHz
Output frequency	2.25 GHz –2.75GHz
Rise Time	76.97 ps
Fall Time	92.73 ps
Power	99.4mW
Power supply	3V

VI. CONCLUSION

The phase modulation of polar transmitter is implemented as demonstrated above. The output waveform of Phase modulation is obtained at the frequency range of 2.25GHz to 2.75GHz at the power dissipation of 99.4mW. The design of the individual blocks such as PLL and its component, SDM and Decimation Filter and Differentiator are implemented, simulated and results of individual blocks are obtained on the Cadence Virtuoso Platform.

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