Various Power Dissipation Techniques for CMOS Inverter

R. Prakash Rao

Abstract: ***Low power design of complex CMOS circuits is one of the major challenges that is being addressed and will be addressed in nanometer design era. With integration of millions and billions of transistors on a single chip, transistor density is drastically increasing that lead to more and more complexity in applications being implemented on a single chip. Design time is another major challenge that forces designers to address the need in a very short time optimizing chip performances. In order to ensure that the design is through in the first iteration, designers are banking on new methodologies and readymade solutions to optimize area, time and power. Hence, various power dissipation techniques for CMOS inverter circuit are investigated here.***

Keywords: Low Power Design, CMOS Circuits, Millions and Billions of Transistors, Transistor Density, Optimize Area, Time and Power.

I. INTRODUTION

1.1. Sources of Power Consumption in VLSI

To measure the power consumption in any CMOS circuits the sources of power consumption should be known. Figure1 represents the sources of power consumed in a CMOS. The major part of the power consumption is Active and Standby power.

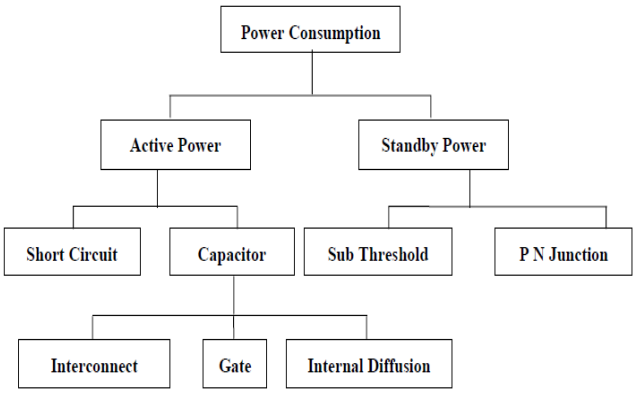

Figure1 Sources of Power Consumption in CMOS Circuits

II. LOW POWER DESIGN TECHNIQUES

Several low power techniques have been reported in the literature for power reduction. At the gate level and circuit level, power reduction is achieved by incorporating additional logic that can control the charging and discharging of current. David Flynn explained about number of power reduction methods that have been used for some time and are also known as mature technologies [1]. The four power different power reduction techniques are (i) Clock gating (ii) Gate level power optimization (iii) Multi Vdd technique (iv) Multi Vt technique

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Dr. R. Prakash Rao, Associate Professor, Department of Electronics and Communication Engineering, Matrusri Engineering College, Saidabad (Hyderabad)-500059, India. E-mail: prakashiits@gmail.com

i) Clock Gating

A significant fraction of dynamic power in chip is in the distribution network of clock. Up to 50 % of dynamic power is spent in clock buffers. The most common way to reduce this power is to turn clocks OFF when they are not required. This approach is known as clock gating as shown in Figure 2. Modern design, support clock gating: they can identify circuits where clock gating can be inserted without changing the function of logic.

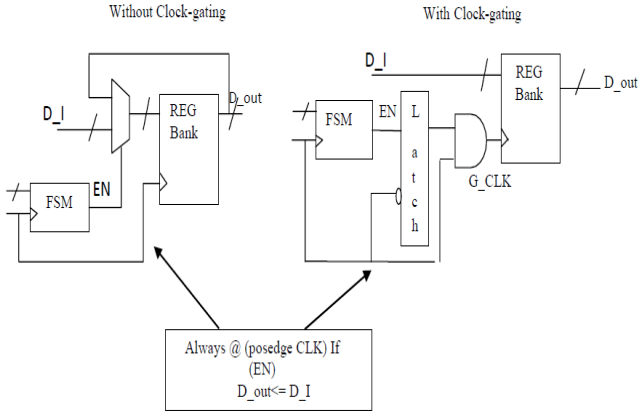

Figure 2. Clock Gating Techniques

An automated clock-gating is performed by identifying synchronous load-enable register banks, and implementing them by gating the clock with an active enable instead of recirculation of the data when the enable is inactive. This technique saves power, and in many cases, saves area as well. At the gate level, optimization of delay, area and static and dynamic power dissipation simultaneously, is required to meet user-defined constraint.

ii) Gate Level Optimization

Energy delay product (power) can be improved by avoiding wastage of energy. This can be done by avoiding number of node transitions that are not necessary. By recording the node transitions in a given circuit for a given input, one can control the power dissipation by minimizing node transitions of the block that consume the maximum power. Most of the times, these blocks are the system clocks and buses. This leads to a significant reduction in the static power. The power dissipation due to short circuit currents is rise/fall times of the input and output signals, can be minimized by matching the rise/fall times of the input and output signal as shown in Figure 3.

iii) Multi V_{dd}

Dynamic power P_{dyn} is proportional to V_{dd}^2 and lowering supply voltage V_{dd} on selected blocks helps to reduce power significantly and also increases

The delay of the gates. The Dynamic power (P_{dyn}) is given by equation (3.7)

$$Pdyn = \alpha * f * C * V_{dd}^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.7)$$

Where α f = Amount of activity as a function of the clock frequency (f)
C = Amount of capacitance being driven/ switched Thus, by reducing the supply voltage the power is also reduced.

iv) Multi Vt

As geometries have shrunk to 130 nm, 90 nm, 65 nm and below, using Multi V_t has become a common way of reducing leakage current. Many libraries today offer two or three version of their cells such as Low V_t, Standard V_t and High V_t. The implementation tools can take advantage of these libraries to optimize timing and power simultaneously. It is now common to use "Dual V_t" flow during synthesis.

The goal of this approach is to minimize the total number of fast, leaky low V_t transistors by deploying them when it is required to meet timing. The design should meet with minimum functionality, before optimizing power, i.e., synthesizing the design with high performance, high leakage library first, and then relaxing back any cells on any critical path by swapping them for their lower performance, lower leakage equivalents [2].

C L Wey presented design of a Parallel multiplier in which time consuming multiplication process is recursively decomposed into simple summation process that can be executed simultaneously. At each recursive step each multiplier and multiplicand is partitioned into four groups of bits and produces 16 partial product terms. An efficient summation process of adding up these partial product terms is proposed[3]. These terms are grouped in accordance with their relative bit position and with the use of two to three counters. In their paper the designs of parallel multipliers implementing various orders of power reduction are also studied.

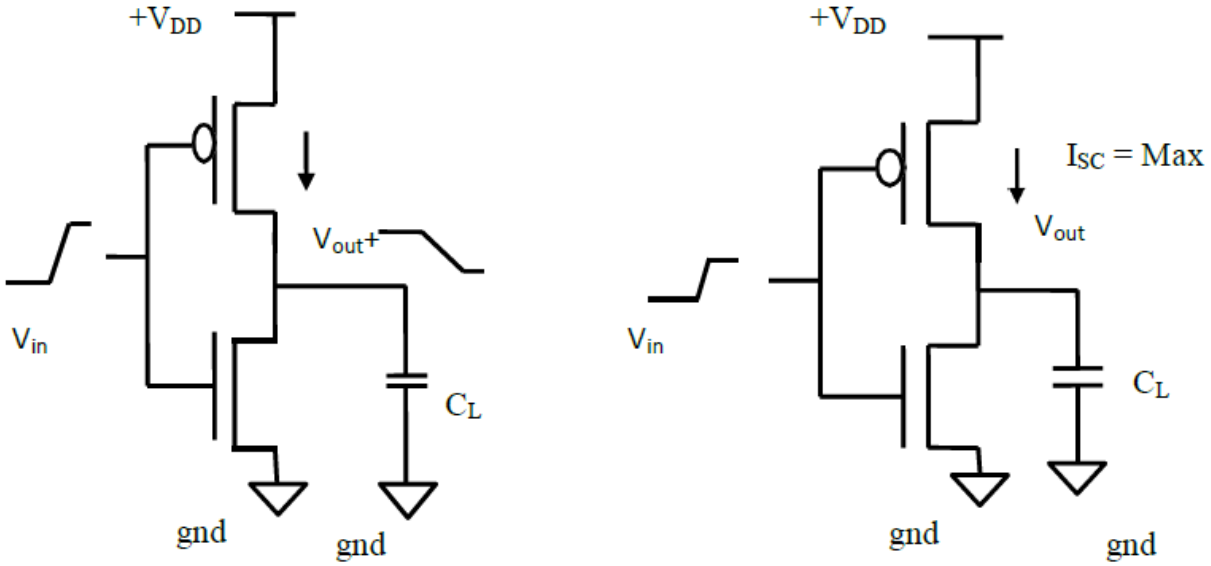

Figure3: Rise/Fall Times on Short-Circuit Currents

In this work, an effort is made to address to reduce power consumption in RRC filter, DUC/DDC and DPLL blocks that are required for 4G communication system by optimizing power at all levels of abstraction. In order to achieve this, power reduction techniques are addressed in designing adders, multiplier and registers required to realize sub-systems[4,5]. Further, these sub-systems are integrated to realize the system; power reduction is also addressed at this level by identifying appropriate number system techniques, selection of architectures and incorporating low power synthesis constraints.

To reduce power further at the transistor level, two techniques are considered; Multi-Vt and Variable Vt technique. The experimental results show average and peak powers obtained for both the techniques by using the HSPICE tool and are listed in Table1.

Table1. Power Dissipations Verses Various Supply Voltages in VTCMOS

Type of Power	V_{dd} = 2.5 V		V_{dd} = 3.3 V		V_{dd} = 1.8 V	
	Active mode	Standby mode	Active mode	Standby mode	Active mode	Standby mode
Average power	$9.1309E^{-2}$	$3.935E^{-13}$	$1.24E^{-3}$	$4.425E^{-13}$	$6.05E^{-4}$	$1.694E^{-13}$
Peak power	$2.05E^{-3}$	$3.393E^{-13}$	$2.79E^{-3}$	$4.26E^{-13}$	$1.34E^{-3}$	$1.695E^{-13}$

Table2 shows average and peak power dissipations obtained in active and stand by modes by varying load capacitance. Table3 shows the power dissipations by varying transistor geometries in VTCMOS.

Table 2. Power Dissipations Verses Load Capacitances in VTCMOS

Type of Power	C_{load}= 0.1 µf		C_{load} = 0.2 µf		C_{load} = 0.3 µf	
	Active mode	Standby mode	Active mode	Standby mode	Active mode	Standby mode
Average power	$6.05E^{-4}$	$1.694E^{-13}$	$6.05E^{-4}$	$4.246E^{-14}$	$6.05E^{-4}$	$4,246E^{-14}$
Peak power	$1.346E^{-3}$	$1.6953E^{-13}$	$1.346E^{-3}$	$4.26E^{-14}$	$1.346E^{-3}$	$4.246E^{-14}$

Table4 shows the average power obtained for various threshold voltages of P- MOS and N-MOS transistors, which reveals as the threshold voltage increases the power dissipation of the circuit decreases.

Table 3. Power Dissipations Verses Transistors Geometries in VTCMOS

Type of Power	W_n/W_p= 0.5		W_n/W_p= 0.4		W_n/W_p= 0.2	
	Active mode	Standby mode	Active mode	Standby mode	Active mode	Standby mode
Average	$6.05E^{-4}$	$1.694E^{-13}$	$5.39E^{-4}$	$1.35E^{-7}$	$5.63E^{-4}$	$1.46E^{-13}$
Peak	1.346E-3	$1.695E^{-13}$	$1.20E^{-3}$	$1.35E^{-3}$	$1.31E^{-3}$	$1.46E^{-13}$

Table5 shows the average power obtained by varying the width-Wn (Wp) for NMOS (PMOS) transistors. Table6 shows the average power obtained for various values of load capacitance. Table7 shows the average power obtained for various values of load supply voltage.

Table 4. Power Obtained Versus Various Threshold Voltages of P- MOS and N-MOS

V_t for NMOS- V	V_t for PMOS- V	Average Power-µW
0.66	-0.66	4.6322
1.66	-1.66	4.1662
2.73	-2.73	3.1154
3.8	-3.8	2.1097
4.8	-4.8	0.6725

Table 5. Power Verses Channel Widths for PMOS and NMOS

W_n for NMOS	W_p for PMOS	Average Power-µW
0.72U	0.36U	5.6559
1.23U	0.61U	9.6382
2.5U	1.25U	18.628
3U	1.5U	22.745
6U	3U	45.187

Table 6. Power Verses Load Capacitance - C_L

Load capacitance (C_L)- pf	Average Power- µW
0.01	5.0245
0.075	5.6625
0.2	5.8077
0.7	5.589
0.9	5.905

Table 7. Average Power Verses Supply Voltage – VDD

V_{DD} – V	Average Power – µW
1.8	1.6616
3.3	3.5464
4	3.9379
4.5	4.891
5	5.596

III. CONCLUSION

From the results presented in Table1 to Table7, the following conclusions are made:

1. Power dissipation occurs in CMOS circuits due to source and sink currents in an inverter not being same and being affected by variations in device geometries, voltage and load.
2. To save power consumption in a transistor, it is required to identify suitable geometry for a given load and power supply.
3. Multi Vt and Variable Vt are the two low power techniques used to further reduce power dissipation at transistor level in a CMOS VLSI circuit.

Based on the review and experimental results discussed in this chapter, it is concluded that, power saving is achieved at transistor level. In order to reduce power dissipation at the higher levels of abstraction it is required to understand the sources of power dissipation and the techniques required to reduce power at levels of hierarchy.

REFERENCES

1. Thomas Olsson, Peter Nilsson, Thomas Meincke (2000), “ADigitally Controlled Low-Power Clock Multiplier for Globally Asynchronous Locally Synchronous Designs”, ISCAS2000, IEEE Int. Symp., Circuits and Systems, Geneva,
2. Fayed. A.A, Bayoumi. M.A (2001), “A novel architecture for low-power design of parallel multipliers”, VLSI Proc., IEEE Computer Society Workshop, pp. 149 – 154, May 2001.
3. In-Chung Hwang, Sang-Hun Song, Soo-Won Kim (2001),“A Digitally Controlled Phase- Locked Loop with a Digital Phase-Frequency Detector for Fast Acquisition”, IEEE JSSC, vol. 36, pp. 1574-1581, Oct.2001.
4. Ming-Chung Tang, R.C. Chang, Wei-Kuan Shih (2001), “Software Radio System Design for Accessing Wireless Multimedia Services”, Int., Journal of Computer Research on Advances in Information Processing and Technology, vol. 10, no. 3, pp. 347 - 360, 2001.
5. John. Proakis (2001), “Digital Communications”, Fourth Edition, Mc.GH. pub
6. Schwarzbacher A.Th., Silvennoinen J.P, Comiskey P.A (2002), “Benchmarking CMOS Adder Structures”, Irish Systems and Signal Conference, Cork, Ireland, pp. 231 – 234, June 2002.